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Data Sheet
July 30, 2026

TEKTRONIX

Tektronix HFS9DG1 Data Time Generator Module

Signal Types: Pulse, NRZ (Non-Return to Zero), RZ (Return to Zero), R1 (Return to One), and DC Phase Lock In Frequency Range: 6 MHz to 630 MHz Output Load: Specified with each channel and complement driving a 50 Ohm load to ground The HFS9DG1 installs in HFS9000 Series mainframes. The HFS9003 provides 3-slot / up to 12-channel capability, and the HFS9009 provides 9-slot / up to 36-channel capability. HFS9DG1 and HFS9DG2 cards can be combined in the same mainframe for mixed logic-family testing. Compared with the HFS9DG2, the HFS9DG1 emphasizes higher bandwidth and fixed fast edges for ECL and GaAs characterization. Phase Lock In Frequency Range: 6 MHz to 630 MHz Output Load: Specified with each channel and complement driving a 50 Ohm load to ground The HFS9DG1 installs in HFS9000 Series mainframes. The HFS9003 provides 3-slot / up to 12-channel capability, and the HFS9009 provides 9-slot / up to 36-channel capability. HFS9DG1 and HFS9DG2 cards can be combined in the same mainframe for mixed logic-family testing. Compared with the HFS9DG2, the HFS9DG1 emphasizes higher bandwidth and fixed fast edges for ECL and GaAs characterization.

MODEL **Tektronix HFS9DG1**	CALIBRATION **Available on request**
CONDITION **Used**	STATUS **In stock**
RFQ / SKU **HFS9DG1**	LISTING **https://aumictechlabs.com/products/hfs9dg1-2/**

NIST-traceable cal · SAM registered · 30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Tektronix HFS9DG1 Data Time Generator Module is a four-channel stimulus card within the HFS9000 Stimulus System, engineered for precise timing signal and data pattern generation in high-speed digital system characterization. This module excels in testing data acquisition and communication systems, with particular strength in ECL and GaAs device characterization. Its high bandwidth and sub-250 ps rise times enable complex test scenario creation across frequency ranges from 50 kHz to 630 MHz.Technical Specifications Output Performance Level resolution: 0.01 V HIGH level accuracy: ±2% of level ±50 mV LOW level accuracy: ±2% of HIGH level ±2% of amplitude ±50 mV Output levels: +5.00 V (maximum HIGH) to -2.50 V (minimum LOW) Peak-to-peak amplitude: 0.01 V to 3.00 V Output transition time (20% to 80%): <250 ps (≤1 Vp-p) Overshoot: +15% +20 mV; Undershoot: -10% -20 mV (200 ps after 50% point) Timing Performance Frequency range: 50 kHz to 630 MHz Frequency resolution: <0.1% of programmed value Frequency accuracy: ±1% of programmed value RMS jitter: 15 ps ±0.05% of interval Channel deskew range: -60 ns to 2.0 µs (1 ps resolution) Delay adjust range: 0 to 20 µs (1 ps resolution, 1% ±50 ps accuracy) Width adjust range: 0 to 65,536 × one period (1 ps resolution, 1% of width ±50 ps accuracy) Phase Lock Input Frequency range: 6 MHz to 630 MHz Amplitude range: 0.8 V to 1.0 Vp-p Output frequency: Any 2n multiple or submultiple of phase lock input frequency (within installed card limits) Trigger Input Input impedance: 50 Ohm Input voltage range: ±5 V maximum Programmable threshold: -4.70 V to +4.70 V (100 mV resolution, ±100 mV ±5% of level accuracy) Minimum pulse width: 1 ns Rise/fall time requirement: <10 ns Sensitivity: <500 mV Interfaces & Control Programmability: GPIB (IEEE 488) Physical & Environmental Dimensions: 51 mm W × 267 mm H × 356 mm D Shipping weight: 1.36 kg Operating temperature: 0°C to +40°C Non-operating temperature: -40°C to +75°C Humidity: up to 95% RH (10–30°C), up to 75% RH (30–40°C) Environmental standard: MIL-T-28800 Type III, Class 5 Line voltage: 90–130 V AC RMS or 180–250 V AC RMSKey Features Four independent stimulus channels per card Sub-250 ps edge placement accuracy for precision timing control 1 ps resolution across deskew, delay, and width adjustment functions Supports complex pattern generation through edge placement manipulation Phase lock capability from 6 MHz to 630 MHz Low jitter performance (15 ps RMS) for sensitive measurementsTypical Applications ECL and GaAs device characterization High-speed digital system stimulus and validation Data acquisition system testing Communication system signal generation Timing and synchronization verificationCompatibility & Integration Operates as a module within the HFS9000 Stimulus System. GPIB control enables integration into automated test environments. Cabinet form factor (51 mm width) supports standard rack mounting configurations.

Features & description

From manufacturer datasheet

Features

• 4 stimulus channels per module • Up to 630 MHz repetition rate • Fixed fast transition time (typically less than or equal to 250 ps, 20% to 80%) • 1 ps timing resolution • Independent edge placement and channel deskew • Signal types: Pulse, NRZ, RZ, R1, and DC • True and complement outputs • Fully digital architecture for flexible edge placement • Ideal for ECL and GaAs device characterization • Modular HFS9000 Series plug-in card

HFS9DG1 Characteristics / Specifications

PARAMETER	VALUE
Model	HFS9DG1
Instrument Type	Data Time Generator Module
System Compatibility	HFS9000 Stimulus System (HFS9003 / HFS9009 mainframes)
Channels	4
Frequency Range	50 kHz to 630 MHz
Frequency Resolution	Less than or equal to 0.1% of frequency setting
Frequency Accuracy	+/-1%
Timing Resolution	1 ps
Channel Deskew Range	-60 ns to 2.0 us
Channel Deskew Resolution	1 ps
Delay Adjustment Range	0 to 20 us
Delay Adjustment Resolution	1 ps
Delay Accuracy	1% of (Lead Delay + Chan Delay) +/-50 ps
Pulse Width Adjustment Range	0 to (one period x 65,536)
Pulse Width Adjustment Resolution	1 ps
Pulse Width Accuracy	1% of width +50 ps, -75 ps
Transition Time (20% to 80%)	Less than or equal to 250 ps for amplitude less than or equal to 1 V; typically about 250 ps for 1 V to 2 V; typically about 260 ps for 2 V to 3 V
Maximum High Level	+5.0 V
Minimum Low Level	-2.5 V
Maximum Amplitude	3.00 V
Minimum Amplitude	0.01 V
Level Resolution	0.01 V
High Level Accuracy	+/-2% of level +/-50 mV
Low Level Accuracy	+/-2% of high level +/-2% of amplitude +/-50 mV

PARAMETER	VALUE
Output Aberrations	Overshoot +15% +20 mV; Undershoot -10% -20 mV
Signal Types	Pulse, NRZ (Non-Return to Zero), RZ (Return to Zero), R1 (Return to One), and DC
Phase Lock In Frequency Range	6 MHz to 630 MHz
Output Load	Specified with each channel and complement driving a 50 Ohm load to ground System Context The HFS9DG1 installs in HFS9000 Series mainframes. The HFS9003 provides 3-slot / up to 12-channel capability, and the HFS9009 provides 9-slot / up to 36-channel capability. HFS9DG1 and HFS9DG2 cards can be combined in the same mainframe for mixed logic-family testing. Compared with the HFS9DG2, the HFS9DG1 emphasizes higher bandwidth and fixed fast edges for ECL and GaAs characterization.
Bandwidth	and fixed fast edges for ECL and GaAs characterization.
Aberrations	Overshoot +15% +20 mV; Undershoot -10% -20 mV

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

performance digital devices.

Applications
The HFS9DG1 is intended for high-speed logic characterization and stimulus applications, including ECL and GaAs device testing, setup and hold margin testing, pattern-sensitivity characterization, and multi-channel synchronous stimulus within HFS9000 mainframes such as the HFS9003 and HFS9009.

Key Features
- 4 stimulus channels per module
- Up to 630 MHz repetition rate
- Fixed fast transition time (typically less than or equal to 250 ps, 20% to 80%)
- 1 ps timing resolution
- Independent edge placement and channel deskew
- Signal types: Pulse, NRZ, RZ, R1, and DC
- True and complement outputs
- Fully digital architecture for flexible edge placement
- Ideal for ECL and GaAs device characterization
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Technical Specifications

Technical Specifications

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PARAMETER	VALUE
	2 V to 3 V
Maximum High Level	+5.0 V
Minimum Low Level	-2.5 V
Maximum Amplitude	3.00 V
Minimum Amplitude	0.01 V
Level Resolution	0.01 V
High Level Accuracy	+/-2% of level +/-50 mV
Low Level Accuracy	+/-2% of high level +/-2% of amplitude +/-50 mV
Output Aberrations	Overshoot +15% +20 mV; Undershoot -10% -20 mV
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System Context

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Operational Notes

Every output can produce data and timing formats, not only simple pulses. Independent voltage levels, widths, and timing relationships can be set per channel. Inactive signals can be held at programmable high or low DC levels, reducing the need for external DC sources and switching.

Notes

This manual OEM source was compiled from Tektronix HFS9000 Series user and service documentation covering the HFS9DG1 Data Time Generator module.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

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