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Data Sheet

August 15, 2026

ACROMAG

Acromag IP-1K100-0024 User-Programmable FPGA Module

Acromag Embedded Test Systems. Frequency Range: 250 kHz to 100 MHz, Voltage / Current Range: 12 V to 32 V DC.



MODEL

Acromag IP-1K100-0024

CALIBRATION

Available on request

CONDITION

Used

STATUS

In stock

RFQ / SKU

IP-1K100-0024

LISTING

<https://aumictechlabs.com/products/ip-1k100-0024-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 • 811210 • 541380

This unit

The Acromag IP-1K100-0024 is a user-programmable FPGA module built around the Altera EP1K100 device for embedded custom logic implementation and high-speed data processing. This Industry Pack (IP) module enables adaptive computing through in-system FPGA configuration via JTAG or IP bus, with a pre-programmed CPLD handling power-up initialization. Engineers develop applications in VHDL using Altera MAX+PLUS® II or Quartus® tools, downloading directly to the FPGA through the IP bus. Technical Specifications FPGA Device: Altera EP1K100 Configuration Interface: JTAG or IP bus with internal CPLD-facilitated initialization Digital I/O Capacity: Up to 48 TTL or 24 EIA-485 signals, or mixed configuration TTL I/O: 5V tolerant; grouped directional control in 8-channel sets Differential I/O: RS485/RS422 transceivers; grouped control in 4-channel sets RS485/RS422 Range: Up to 32 nodes over 4000 feet of cable IP Bus Clock: 8 MHz and 32 MHz operation IP Bus Standard: ANSI/VITA 4-1995 compliant ID Space Read Access (8

MHz): 0 wait states, 250 ns cycle time Register Read/Write Access (8 MHz): 1 wait state, 500 ns cycle time Data Widths: 8-bit ID space; 8 or 16-bit I/O space Interrupt Support: Two IP request levels Clock Synthesizer: PLL-based, programmable 250 kHz to 100 MHz output External Clock Input: LVTTTL with direct FPGA global clock connection Interval Timer: User-programmable Power Input: 12 V to 32 V DC with reverse-polarity protection Operating Temperature: -40°C to +60°C ambient

Key Features In-system reprogrammable logic via standard JTAG interface Flexible I/O mixing of TTL and differential signals Wide-range DC power input with reverse-polarity protection Programmable clock synthesis from 250 kHz to 100 MHz Support for specialized EIA-422/485 communication networks Extended temperature operation from -40°C to +60°C

Typical Applications Specialized communication systems over EIA-422/485 networks Signal simulation over TTL-switched lines Advanced data analysis and custom signal processing Adaptive computing requiring field-programmable logic

Compatibility & Integration The module conforms to ANSI/VITA 4-1995 IP bus specifications and integrates with standard FPGA design flows. DMA is wired to the FPGA but not supported in the provided example firmware.

IP1K1000024 Characteristics / Specifications

PARAMETER	VALUE
Model	IP-1K100
Configuration Example	IP-1K100-0024 24 differential EIA-485
Instrument Type	user programmable FPGA IndustryPack
Fpga Device	Altera ACEX EP1K100
Typical Gates	100000
Maximum System Gates	257000
Logic Elements	4992
Embedded Array Blocks	12
Total Ram Bits	49152
Ttl Io Maximum	48
Eia485 Io Maximum	24
Ip Bus Rates	8 MHz and 32 MHz
Form Factor	single-wide IndustryPack
Download Path	IP bus into FPGA
Power Up Controller	preprogrammed CPLD then FPGA takes IP bus
Io Mix	TTL and EIA-485 combinable
Timer	user programmable interval timer
Clock	programmable PLL synthesizer
Carrier Bus	IndustryPack
Use Case	adaptive computing mezzanine
Manufacturer	Acromag
Related Module	IP-1K110 reconfigurable FPGA IP
Core Voltage Class	2.5 V ACEX 1K
Process Class	0.22/0.18 um hybrid ACEX
Registers Class	5319 on EP1K100

PARAMETER	VALUE
Jtag Ir Length Class	10 on EP1K100
Operating Use	EIA-485 networks and TTL simulation

IP1K1000024 Specifications

PARAMETER	VALUE
Applications	Custom EIA-422/485 communications, TTL test-fixture simulation, and FPGA-based math/DSP on IndustryPack carriers.
Key Features	Altera EP1K100 ACEX FPGA
Technical Specifications	Model: IP-1K100

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
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Operating Use	EIA-485 networks and TTL simulation
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Notes

From Acromag IP-1K100 product description and Altera ACEX EP1K100 device table (gates, LEs, RAM). IP-1K100-0024 is the 24-line EIA-485 configuration. Carrier electricals follow the IP specification.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.