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Data Sheet
August 15, 2026

ACROMAG

Acromag IP-EP201 JTAG-Reconfigurable Cyclone II FPGA Digital I/O Module

Acromag Digital Input Board. Frequency Range: 250 kHz to 100 MHz, Voltage / Current Range: 5V tolerant TTL I/O.

MODEL Acromag IP-EP201	CALIBRATION Available on request
CONDITION Used	STATUS In stock
RFQ / SKU IP-EP201	LISTING https://aumictechlabs.com/products/ip-ep201-2/

NIST-traceable cal · SAM registered · 30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Acromag IP-EP201 is an Industry Pack (IP) module that delivers 48 TTL bidirectional digital I/O lines through a JTAG-reconfigurable Altera Cyclone II FPGA. Designed for industrial digital interfacing, this module combines user-programmable logic with direct FPGA control and flexible clocking, enabling custom I/O solutions without external interface logic.Technical Specifications FPGA Core Altera Cyclone II EP2C20 JTAG or IP bus configuration download Digital I/O 48 TTL bidirectional I/O lines, 5V tolerant LVTTL external clock input connected directly to FPGA global clock pin Direction control in 8-channel groups Clocking On-board Cypress CY22150 clock synthesizer (or equivalent) Frequency range: 250 kHz to 100 MHz IP bus clock support: 8 MHz and 32 MHz IP Bus Interface ANSI/VITA 4-1995 compliant 8 or 16-bit I/O space data width 8-bit ID space Access time (8 MHz): 1 wait state, 375 nS cycle Two interrupt request levels Wired DMA support (not enabled in example firmware) Power-Up & Configuration On-board CPLD manages

boot and FPGA download FPGA assumes full IP bus control post-configuration Environmental Operating temperature: 0 to 70°C (standard); -40 to 85°C (IP-EP201E extended range) Storage temperature: -55 to 125°C Humidity: 5 to 95% non-condensingKey Features User-programmable logic via Altera Quartus II tools and VHDL Rapid I/O reconfiguration without hardware redesign Global clock distribution for timing-critical applications Independent channel direction control enables mixed input/output configurationsTypical Applications Digital signal acquisition, real-time control interfaces, test automation, industrial protocol bridging, and custom instrumentation requiring flexible I/O expansion.Compatibility & Integration Engineering Design Kit includes schematics, parts list, and example VHDL code. Requires VHDL expertise and Altera Quartus II development environment.

IPEP201 Characteristics / Specifications

PARAMETER	VALUE
Model	IP-EP201
Instrument Type	Reconfigurable FPGA IndustryPack module
Fpga	Altera Cyclone II EP2C20
Ttl Lines	48 TTL I/O (IP-EP201)
Sibling Rs4	IP-EP202 24 differential RS485
Sibling Mixed	IP-EP203 24 TTL and 12 RS485
Sibling Lvds	IP-EP204 24 LVDS
Local Sram	64K x 16 under FPGA control
Clock Synthesizer	Cypress CY22150 or equivalent 250 kHz to 100 MHz
External Clock	LVTTL external clock into the FPGA
Ip Bus Clock	8 MHz and 32 MHz supported
Id Space	8-bit data
Io Space	8 or 16-bit data
Interrupt Levels	two IP request levels
Ip Standard	ANSI/VITA 4-1995
Id Access Time	1 wait state 375 ns cycle at 8 MHz
Register Access Time	1 wait state 375 ns cycle at 8 MHz
Interrupt Access Time	1 wait state 375 ns cycle at 8 MHz
Operating Temperature Standard	0 to 70 C
Operating Temperature E	minus 40 to 85 C (IP-EP201E)
Storage Temperature	minus 55 to 125 C
Humidity	5 to 95 percent non-condensing
Configuration Path	JTAG port or IP bus download
Edk	IP-EP2-EDK engineering design kit required for first FPGA development
Manufacturer	Acromag

PARAMETER	VALUE
Mechanical Package	single-size IndustryPack
Operating temperature	Standard: 0 to 70 C

General Specifications & Supplementary Characteristics

PARAMETER	VALUE
Storage temperature	minus 55 to 125 C
Operating temperature	Standard: 0 to 70 C
Operating Temperature	Standard: 0 to 70 C
Humidity	5 to 95 percent non-condensing
Operating Temperature Standard	0 to 70 C
Operating Temperature E	minus 40 to 85 C (IP-EP201E)
Configuration Path	JTAG port or IP bus download
Edk	IP-EP2-EDK engineering design kit required for first FPGA development
Manufacturer	Acromag
Mechanical Package	single-size IndustryPack Notes From Acromag IP-EP200 JTAG-Reconfigurable Cyclone II FPGA Digital I/O Modules datasheet (8400463). IP-EP201 is the 48-TTL I/O model; confirmEtemperature suffix.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

PARAMETER	VALUE
Model	IP-EP201
Instrument Type	Reconfigurable FPGA IndustryPack module
Fpga	Altera Cyclone II EP2C20
Ttl Lines	48 TTL I/O (IP-EP201)
Sibling Rs485	IP-EP202 24 differential RS485
Sibling Mixed	IP-EP203 24 TTL and 12 RS485
Sibling Lvds	IP-EP204 24 LVDS
Local Sram	64K x 16 under FPGA control
Clock Synthesizer	Cypress CY22150 or equivalent 250 kHz to 100 MHz
External Clock	LVTTL external clock into the FPGA
Ip Bus Clock	8 MHz and 32 MHz supported
Id Space	8-bit data
Io Space	8 or 16-bit data
Interrupt Levels	two IP request levels
Ip Standard	ANSI/VITA 4-1995
Id Access Time	1 wait state 375 ns cycle at 8 MHz
Register Access Time	1 wait state 375 ns cycle at 8 MHz
Interrupt Access Time	1 wait state 375 ns cycle at 8 MHz
Operating Temperature Standard	0 to 70 C
Operating Temperature E	minus 40 to 85 C (IP-EP201E)
Storage Temperature	minus 55 to 125 C
Humidity	5 to 95 percent non-condensing
Configuration Path	JTAG port or IP bus download
Edk	IP-EP2-EDK engineering design kit required for first FPGA development
Manufacturer	Acromag

PARAMETER	VALUE
Mechanical Package	single-size IndustryPack

Notes
From Acromag IP-EP200 JTAG-Reconfigurable Cyclone II FPGA Digital I/O Modules datasheet (8400463). IP-EP201 is the 48-TTL I/O model; confirmEtemperature suffix.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

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