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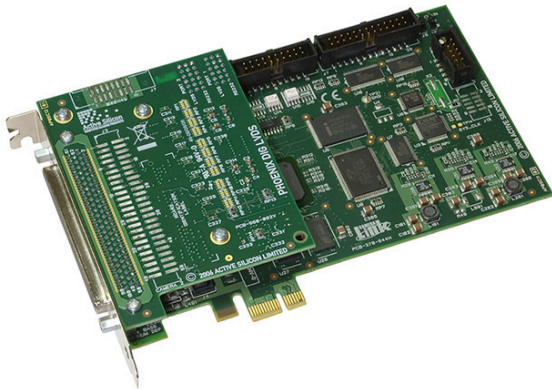
Data Sheet

August 15, 2026

ACTIVE SILICON

Active Silicon Phoenix-D36-PE1 LVDS Digital Frame Grabber

Active Silicon Data Acquisition Systems (DAQ). Frequency Range: 60 MHz maximum pixel clock, Voltage / Current Range: +3.3V @ 1A.



MODEL

**Active Silicon
Phoenix-D36-PE1**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

Phoenix-D36-PE1

LISTING

<https://aumictechlabs.com/products/phoenix-d36-pe1-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Active Silicon Phoenix-D36-PE1 is a PCI Express digital frame grabber designed for high-speed image acquisition in industrial, medical, and scientific applications. It captures digital data from frame and line scan cameras via LVDS and RS-422 interfaces, delivering burst rates exceeding 190 MBytes/sec over a single-lane PCIe v1.1 connection. The board employs an FPGA for flexible, software-configurable interfacing and includes hardware-accelerated DataMapper for real-time reformatting of camera data. Technical Specifications Data Interface: 36-bit EIA-644 (LVDS) inputs plus 4 dedicated control bits (Frame Enable, Line Enable, Data Enable, Pixel Clock) Pixel Clock: Maximum 60 MHz Data Width Support: Single 12-bit RGB or 32-bit mono; multi-tap configurations; alternative mode supports two independent 16-bit mono cameras Mono Data Widths: 8-, 10-, 12-, 14-, 16-, or 32-bit Color Data Widths: 15-, 16-, 24-, 32-, or 48-bit RGB/BGR Camera Tap Formats: Line interlaced, line offset, pixel interlaced, pixel offset PCI Express: Single-

lane (x1) v1.1; burst rates exceed 190 MBytes/sec Bus Mastering: 0% CPU utilization for scatter-gather operations Power Consumption: +3.3V at 1A typical

Key Features

Hardware DataMapper converts raw camera data on-card, including mono-to-32-bit color conversion Region of Interest (ROI) and sub-sampling controls optimize processing speed Dual UART channels support EIA-232 (RS-232) and EIA-644 (LVDS) signaling 4-bit opto-isolated I/O with configurable input/output allocation; outputs sink 20 mA from 24V; inputs sense 3.3V to 24V as logic high Two 2-bit differential LVDS input ports (AuxInXY) for external devices such as shaft encoders Two 8-bit TTL I/O ports FPGA-based 16-bit input, 16-bit lookup table (LUT) for custom processing

Typical Applications Machine vision, automated inspection, medical imaging, scientific research, and industrial quality control requiring flexible multi-camera acquisition and on-board data conditioning.

Compatibility & Integration Supports multi-tap and single-tap camera architectures with line and pixel interlacing. Compatible with standard frame and line scan cameras using LVDS control and data signaling. End-of-life product; contact sales for alternative solutions.

PHOENIXD36PE1 Characteristics / Specifications

PARAMETER	VALUE
Model	Phoenix-D36-PE1
Instrument Type	PCI Express LVDS digital frame grabber
Family	Active Silicon Phoenix-D36
Host Bus	PCI Express 1.1 single lane (x1), max payload 512 bytes
Burst Rate	greater than 190 Mbyte/s posted writes
Data Width	36 bit EIA-644 plus 4 control bits
Pixel Clock	DC to 60 MHz, programmable polarity
Channel Split	two 20-bit LVDS channels, 16 data + 4 control each
Rgb Mode	12-bit RGB (36-bit) or up to 32-bit mono
Pci Fifo	4096 by 32 bit
Lut	16 bit in / 16 bit out, 65536 by 16 per channel
Address Space	16 MByte memory plus 256 byte I/O
Uart	dual channel, 300 to 115200 baud, 5-8 data bits, 64-char HW FIFOs
Opto Io	4 bits, standard 2 in / 2 out, 20 mA sink, 24 V off, 3.3-24 V in
Ttl Io	two 8-bit ports, 24 mA source at min 2.2 V / sink at max 0.55 V
Camera Connector	100-way mini-D Honda PCS-XE100LFD-HS, 4-40 UNC
Pcb Size	143 mm by 111 mm
Overall Size	174 mm by 127 mm including bracket and connectors
Mass	approximately 150 g
Supply	+3.3 V, 1 A typical
Operating Temperature	0 C to plus 55 C
Storage Temperature	minus 15 C to plus 70 C
Humidity	10 to 90 percent non-condensing
Emc	EN 55022:1998 Class A, EN 55024:1998, FCC Class AFlammability: 94-V0
Manufacturer	Active Silicon

PARAMETER	VALUE
Literature	Phoenix-D36 PCI Express PE1 datasheet AS-PHX-D36-PE1

General Specifications & Supplementary Characteristics

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Literature	Phoenix-D36 PCI Express PE1 datasheet AS-PHX-D36-PE1 Notes From Active Silicon Phoenix-D36 PE1 datasheet. PE4 is the x4 sibling with greater than 750 MB/s and isadifferent SKU.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
Technical Specifications	
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Pci Fifo	4096 by 32 bit
Lut	16 bit in / 16 bit out, 65536 by 16 per channel
Address Space	16 MByte memory plus 256 byte I/O
Uart	dual channel, 300 to 115200 baud, 5-8 data bits, 64-char HW FIFOs
Opto Io	4 bits, standard 2 in / 2 out, 20 mA sink, 24 V off, 3.3-24 V in
Ttl Io	two 8-bit ports, 24 mA source at min 2.2 V / sink at max 0.55 V
Camera Connector	100-way mini-D Honda PCS-XE100LFD-HS, 4-40 UNC
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Notes
From Active Silicon Phoenix-D36 PE1 datasheet. PE4 is the x4 sibling with greater than 750 MB/s and isadifferent SKU.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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<https://aumictechlabs.com>

NIST-traceable calibration · SAM registered ·
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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.