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Data Sheet

August 15, 2026

AGILENT / KEYSIGHT

Agilent/Keysight 1661CS

HP Agilent 1661CS Benchtop Logic Analyzer 102 Channel with Oscilloscope The HP 1661CS is a 102-channel 1660CS-series benchtop logic analyzer with a built-in 2-channel oscilloscope. OEM 1660C/CS/CP technical data list 100 MHz state on all channels, 250 MHz conventional timing (500 MHz half-channel), 4K memory (8K half-channel), 6 state clocks/qualifiers, and a 1 GSa/s 250 MHz 8-bit scope with 8k samples per channel. Hardware timing, processor mnemonics, and analog parametric measurements on embedded systems. The HP 1661CS is a 102-channel 1660CS-series benchtop logic analyzer with a built-in 2-channel oscilloscope. OEM 1660C/CS/CP technical data list 100 MHz state on all channels, 250 MHz conventional timing (500 MHz half-channel), 4K memory (8K half-channel), 6 state clocks/qualifiers, and a 1 GSa/s 250 MHz 8-bit scope with 8k samples per channel. Hardware timing, processor mnemonics, and analog parametric measurements on embedded systems. Integrated 2-channel 1 GSa/s oscilloscope 100 MHz state / 500 MHz half-channel timing



MODEL

**Agilent / Keysight
1661CS**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

1661CS

LISTING

<https://aumictechlabs.com/products/1661cs-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Agilent/Keysight 1661CS is a portable benchtop logic analyzer combining state and timing analysis with integrated oscilloscope capabilities for digital system verification and debugging. It captures and analyzes complex digital signals across embedded systems, ASICs, and custom digital designs using deep memory, multi-level sequencing, and flexible triggering to isolate

events in extended capture windows. Technical Specifications Channels & Memory 102 data channels 6 clock/data channels State analysis: 4K states per channel; 8K states in half-channel mode State Analysis Operating speed: 100 MHz Timing Analysis Conventional: 250 MHz (all channels), 500 MHz (half channels) Transitional: 125 MHz (all channels), 250 MHz (half channels) Glitch detection: 125 MHz (half channels) Timing resolution: 2 ns Integrated Oscilloscope 2 channels at 1 GSa/s sampling rate 250 MHz bandwidth (single shot) 8000 samples per channel memory Automatic pulse parameters and time interval measurements with statistical marker analysis Triggering 12-level sequencing (state analysis) 10-level sequencing (timing analysis) Digital trigger capabilities Storage & Interfaces 540 MB internal hard disk drive 3.5-inch flexible disk drive Ethernet LAN (optional ThinLAN and Ethertwist ports) RS-232-C serial HP-IB Centronics printer interface Key Features Dual analysis modes enable both synchronous state capture and asynchronous timing measurements in a single instrument. The 2 ns timing resolution supports high-speed signal verification. CRT display with mouse control and optional keyboard provides intuitive navigation across large capture datasets. Typical Applications Embedded system debugging, ASIC functional verification, digital signal troubleshooting, and timing margin analysis in processor-based designs. Compatibility & Integration Supports HP B3740A software analyzer for source-level correlation with C++ code and inverse assembly. Processor-specific mnemonics and inverse assemblers available for popular microprocessor families. Over 200 probe solutions support diverse connection topologies. User interface aligns with HP 16500 system architecture.

1661CS Characteristics / Specifications

PARAMETER	VALUE
Model	1661CS
Instrument Type	Benchtop logic analyzer with oscilloscope
State And Timing Channels	102
Data Channels	96 data plus 6 clock/data
State Analysis Speed	100 MHz all channels
Timing Conventional Full	250 MHz all channels
Timing Conventional Half	500 MHz half channels
Timing Transitional Full	125 MHz all channels
Timing Transitional Half	250 MHz half channels
Glitch Timing	125 MHz half channels
State Clocks Qualifiers	6
Memory Depth Full	4K per channel
Memory Depth Half	8K per channel
Scope Channels	2
Scope Sample Rate	1 GSa/s per channel
Scope Bandwidth	dc to 250 MHz dc coupled
Scope Rise Time	1.4 ns
Scope Vertical Resolution	8 bits
Scope Memory	8k samples per channel
Mass Storage	3.5 inch floppy plus 540 MB hard disk
Remote Interfaces	HP-IB RS-232 Centronics
Lan	code 015 on C/CS; standard on CP
Manufacturer	HP Agilent Keysight
Bandwidth	dc to 250 MHz dc coupled
Rise Time	1.4 ns

1661CS Specifications

PARAMETER	VALUE
Applications	Hardware timing, processor mnemonics, and analog parametric measurements on embedded systems.
Key Features	102 state and timing channels
Technical Specifications	Model: 1661CS

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

technical data list 100 MHz state on all channels, 250 MHz conventional timing (500 MHz half-channel), 4K memory (8K half-channel), 6 state clocks/qualifiers, and a 1 GSa/s 250 MHz 8-bit scope with 8k samples per channel.

Applications

Hardware timing, processor mnemonics, and analog parametric measurements on embedded systems.

Key Features

102 state and timing channels

Integrated 2-channel 1 GSa/s oscilloscope

100 MHz state / 500 MHz half-channel timing

HP-IB RS-232 and Centronics standard

Optional LAN (code 015) on C/CS models

Technical Specifications

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Notes

From HP 1660C/CS/CP-series benchtop logic analyzer technical data, 1661CS column, plus 1660CS user's guide channel counts. 1661C is the analyzer-only sibling without the scope.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.