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Data Sheet
August 14, 2026

AGILENT / KEYSIGHT

Agilent/Keysight 81250A – ParBERT Platform Mainframe

Agilent 81250A ParBERT Parallel Bit Error Ratio Tester The Agilent 81250 ParBERT isamodular parallel electrical and optical BER test platform. OEM 5968-9188E lists modules at 675 Mb/s, 1.65 Gb/s, 2.7 Gb/s, 3.35 Gb/s, 7 Gb/s, 10.8 Gb/s, 13.5 Gb/s and 45 Gb/s with PRWS, PRBS to 2^31-1, and user-defined patterns. SerDes, mux/demux, 10GbE, FEC, and parallel-to-serial BER characterization in VXI-based ATE. Modular generator and analyzer mix of speed classes

MODEL **Agilent / Keysight 81250A**	CALIBRATION **Available on request**
CONDITION **Used**	STATUS **In stock**
RFQ / SKU **81250A**	LISTING **https://aumictechlabs.com/products/81250a-2/**

NIST-traceable cal · SAM registered · 30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Agilent/Keysight 81250A is a modular parallel bit error ratio tester (BERT) platform engineered for characterization of high-speed multi-port devices across computing, telecommunications, and semiconductor applications. Built on a VXI mainframe architecture, the system accommodates plug-in modules for flexible, scalable configurations. It performs both electrical and optical signal generation and analysis across data rates from 675 Mbit/s to 45 Gbit/s.Technical Specifications Data Rate Support: 675 Mbit/s, 1.65 Gbit/s, 2.7 Gbit/s, 3.35 Gbit/s, 7 Gbit/s, 10.8 Gbit/s, 13.5 Gbit/s, 45 Gbit/s (via dedicated modules) Clocking and Timing: External clock input: up to 10.8/21.6 GHz Central clock modules include E4805B (675 MHz), E4808A (high performance), and E4809A (13.5 GHz) Example timing (E4866A 10.8 Gb/s generator): data range 9.5–10.8 Gbit/s, clock range 9.5–

10.8 GHz, delay range 0–300 ns, delay resolution 1 ps, accuracy ±20 ps ±50 ppm relative to zero-delay Module skew: typically 50 ps after deskewing for same-type modules at unchanged system frequency Delay control input for jitter generation Sub-rate clock outputs available Pattern Generation and Analysis: Pseudo-Random Word Sequences (PRWS), PRBS, and user-defined patterns on parallel lines Memory-based patterns: 256-bit segment length resolution, up to 33,554,432 bits Multi-level signal generation via internal digital and analog channel add functions Pattern sequencing for data flow control (single, looped, infinite) Event handling for real-time control with external signal integration (stop/go, loop control, error triggering) Bit error ratio analysis with user-defined, PRBS/PRWS, or mixed data System Architecture: Master-slave clock configurations for synchronized multi-frame operation Clock Data Recovery (CDR) available in select modules (e.g., 45 Gb/s DeMUX) Multiple clock groups supporting asynchronous or synchronized operationKey Features Modular VXI mainframe design for scalable single-module to multi-mainframe configurations Multi-port parallel testing capability Electrical and optical signal support Flexible clocking with external inputs to 21.6 GHzTypical Applications High-speed device characterization in computer and telecommunications sectors Semiconductor test and validation Multi-port parallel data path verification Jitter and timing analysisCompatibility & Integration The platform integrates dedicated plug-in modules for specific data rates and functions. Clock synchronization across multiple frames enables large-scale parallel test systems. Event-triggered logic supports integration with automated test environments.

81250A Characteristics / Specifications

PARAMETER	VALUE
Model	81250A
Instrument Type	Parallel bit error ratio tester platform
Series Family	Agilent ParBERT 81250
Maximum Serial Data Rate	45 Gb/s (ParBERT 43/45G)
Parallel Data Rate Max	13.5 Gbit/s generator and analyzer channels
Speed Class 6	333.334 kb/s to 675 Mb/s (E4832A back-end class)
Speed Class 16	333.334 Mb/s to 1.65 Gb/s class
Speed Class 27	333.334 Mb/s to 2.7 Gb/s class
Speed Class 33	20.834 Mb/s to 3.35 Gb/s class
Speed Class 7G	620 Mb/s to 7 Gb/s (N4874A generator, N4875A analyzer)
Speed Class 1	620 Mb/s to 13.5 Gb/s (N4872A generator, N4873A analyzer)
Max Channels 6	up to 132 generator/analyzer channels at 675 Mbit/s
Max Channels 33	up to 66 channels at 1.65, 2.7, or 3.35 Gbit/s
Max Channels 1	up to 30 channels at 7 Gbit/s or 13.5 Gbit/s
Memory Depth Per Channel	up to 64 Mbit
Prbs Patterns	hardware PRBS/PRWS up to 2^31-1 plus 2^15-1 and 2^23-1
Pattern Formats	NRZ, DNRZ, RZ, R1
Detect Word	48 bit detect word or pure PRBS without detect word on N4873A/N4875A class
Clock Module 1	E4809A 13.5 GHz central clock, two VXI slots
Cable Reference	specifications valid at end of N4910A 24 inch matched pair 2.4 mm cable unless otherwise stated
Generator Module Width 1	N4872A one VXI slot
Analyzer Module Width 1	N4873A one VXI slot
Host Form Factor	VXI mainframe modular system
Data Rate	45 Gb/s (ParBERT 43/45G)

81250A Specifications

PARAMETER	VALUE
Agilent 81250A ParBERT Parallel Bit Error Ratio Tester	Overview
Applications	SerDes, mux/demux, 10GbE, FEC, and parallel-to-serial BER characterization in VXI-based ATE.
VXI mainframe architecture with central clock modules	Eye opening, fast eye mask, and DUT timing/jitter measurements
Technical Specifications	Model: 81250A

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

PARAMETER	VALUE
Model	81250A
Instrument Type	Parallel bit error ratio tester platform
Series Family	Agilent ParBERT 81250
Maximum Serial Data Rate	45 Gb/s (ParBERT 43/45G)
Parallel Data Rate Max	13.5 Gbit/s generator and analyzer channels
Speed Class 675	333.334 kb/s to 675 Mb/s (E4832A back-end class)
Speed Class 1650	333.334 Mb/s to 1.65 Gb/s class
Speed Class 2700	333.334 Mb/s to 2.7 Gb/s class
Speed Class 3350	20.834 Mb/s to 3.35 Gb/s class
Speed Class 7G	620 Mb/s to 7 Gb/s (N4874A generator, N4875A analyzer)
Speed Class 135	620 Mb/s to 13.5 Gb/s (N4872A generator, N4873A analyzer)
Max Channels 675	up to 132 generator/analyzer channels at 675 Mbit/s
Max Channels 3350	up to 66 channels at 1.65, 2.7, or 3.35 Gbit/s
Max Channels 108	up to 33 channels at 10.8 Gbit/s
Max Channels 135	up to 30 channels at 7 Gbit/s or 13.5 Gbit/s
Memory Depth Per Channel	up to 64 Mbit
Prbs Patterns	hardware PRBS/PRWS up to 2^31-1 plus 2^15-1 and 2^23-1
Pattern Formats	NRZ, DNRZ, RZ, R1
Detect Word	48 bit detect word or pure PRBS without detect word on N4873A/N4875A class
Clock Module 135	E4809A 13.5 GHz central clock, two VXI slots
Cable Reference	specifications valid at end of N4910A 24 inch matched pair 2.4 mm cable unless otherwise stated
Generator Module Width 135	N4872A one VXI slot
Analyzer Module Width 135	N4873A one VXI slot
Host Form Factor	VXI mainframe modular system

Notes

Numeric platform rows from Agilent ParBERT 81250 Parallel Bit Error Ratio Tester data sheet 5968-9188E and the 81250 system user-guide module table. Installed front-end/module mix sets the actual rate and channel count.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

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Generated August 14, 2026