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Data Sheet

August 14, 2026

AGILENT / KEYSIGHT

Agilent / Keysight 83496B Clock Recovery Module With Phase Noise Analysis

Agilent Keysight 83496B Clock Recovery Module 50 Mb/s to 14.2 Gb/s The Keysight 83496B is an 86100C/D clock-recovery plug-in. OEM 86100D configuration guide lists 50 Mb/s to 7.1 Gb/s standard, Option 200 50 Mb/s to 14.2 Gb/s, Option 201 7.1 to 14.2 Gb/s, Option 300 tunable loop-bandwidth golden PLL, Option 100 electrical taps, and Option 101 SM (1260-1360 and 1490-1600 nm) plus MM (830-860 and 1260-1360 nm) optical with electrical inputs. Triggering DCA eyes on 10GbE, 8GFC, and 14 Gb/s-class electrical/optical data; golden-PLL jitter measurements with Option 300. The Keysight 83496B is an 86100C/D clock-recovery plug-in. OEM 86100D configuration guide lists 50 Mb/s to 7.1 Gb/s standard, Option 200 50 Mb/s to 14.2 Gb/s, Option 201 7.1 to 14.2 Gb/s, Option 300 tunable loop-bandwidth golden PLL, Option 100 electrical taps, and Option 101 SM (1260-1360 and 1490-1600 nm) plus MM (830-860 and 1260-1360 nm) optical with electrical inputs. Triggering DCA eyes on 10GbE, 8GFC, and 14 Gb/s-class electrical/optical data; golden-PLL jitter measurements with Option 300.



MODEL

**Agilent / Keysight
83496B**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

83496B

LISTING

<https://aumictechlabs.com/products/83496b-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Agilent/Keysight 83496B Clock Recovery Module extracts clock signals from high-speed data streams and performs phase noise analysis integrated with the Keysight 86100C Digital Communications Analyzer. It recovers clocks from Non-Return-to-Zero (NRZ) signals with residual jitter under 300 femtoseconds RMS at jitter-free input, enabling precise eye-mask and jitter measurements across a wide operating range. The module supports flexible PLL configuration with tunable loop bandwidth and includes pre-configured compliance tests for PCI Express and SONET/SDH applications.

Technical Specifications

Clock Recovery Data rate range: 50 Mb/s to 14.21 Gb/s (continuous tuning) Option 200: 50 Mb/s to 14.2 Gb/s Option 201: 7.1 Gb/s to 14.2 Gb/s Option 100 (electrical): 50 Mb/s to 7.1 Gb/s

Signal types: NRZ

Residual jitter: < 300 femtoseconds RMS (jitter-free input)

PLL and Jitter Analysis Loop bandwidth tuning: 15 kHz to 10 MHz (Option 300) Fixed bandwidth options: 270 kHz or 1.5 MHz

Golden PLL operation with high gain for spread-spectrum tracking

Jitter spectrum and phase noise analysis via external application

Fast, accurate, repeatable jitter transfer and PLL bandwidth measurements

Electrical Interface (Option 100) Input connectors: 3.5 mm (m), single-ended or differential

Minimum electrical input level: 75 mVpp

Output connectors: 3.5 mm (m), single-ended or differential

Key Features

- Integrated phase noise analysis for signal characterization
- Pre-configured PCI Express approved PLL bandwidth compliance tests
- SONET/SDH jitter transfer measurement with automatic report generation
- Tunable loop bandwidth for optimized jitter transfer performance
- High gain PLL tracking for spread-spectrum signal recovery

Typical Applications

- High-speed communication system characterization
- Component performance optimization in R&D and manufacturing
- PLL bandwidth and jitter transfer compliance testing
- Phase noise and jitter spectrum analysis

Compatibility & Integration

Integrates with Keysight 86100C Digital Communications Analyzer. Multiple configurations support electrical and optical applications across diverse data rates and signal types.

83496B Characteristics / Specifications

PARAMETER	VALUE
Instrument Type	Clock recovery plug-in module
Series Family	Keysight 83496B / 86100 DCA
Standard Operating Range	50 Mb/s to 7.1 Gb/s
Host Mainframe	86100C/D (not 86100A/B)
Etr Recommendation	86100D-ETR recommended with 83496x modules
Str Cable	external cable 5062-6690 class from module trigger/clock output to 86100D trigger if Option STR
Form Factor	86100 plug-in
Function	recovered clock for oscilloscope trigger
Predecessor	83496A
Literature	Keysight 86100D DCA configuration guide 5992-0038
Operating Temperature Family	plus 10 C to plus 40 C class of 86100 modules
Application	10 Gb/s-class eyes and jitter with golden PLL
Output	recovered electrical clock
Input	optical SM/MM and/or electrical per option
Firmware	86100C/D required
Bandwidth	golden PLL
Data Rate	0.05 to 14.2 Gb/s upgrade
Operating temperature	Family: plus 10 C to plus 40 C class of 86100 modules

83496B Specifications

PARAMETER	VALUE
Applications	Triggering DCA eyes on 10GbE, 8GFC, and 14 Gb/s-class electrical/optical data; golden-PLL jitter measurements with Option 300.
Key Features	Continuous 50 Mb/s to 7.1 or 14.2 Gb/s
Integrated signal taps	Option 300 adjustable loop BW
Technical Specifications	Instrument Type: Clock recovery plug-in module

General Specifications & Supplementary Characteristics

PARAMETER	VALUE
Operating temperature	Family: plus 10 C to plus 40 C class of 86100 modules
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Application	10 Gb/s-class eyes and jitter with golden PLL
Output	recovered electrical clock
Input	optical SM/MM and/or electrical per option
Firmware	86100C/D required Notes Numeric rate and wavelength rows from Keysight 86100D Infiniium DCA-X configuration guide 5992-0038 (83496B option table). Residual jitter of the CDR itself is in the 83496B specification table of the 86100 module data sheet.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
Specifications	
PARAMETER	VALUE
Instrument Type	Clock recovery plug-in module
Series Family	Keysight 83496B / 86100 DCA
Standard Operating Range	50 Mb/s to 7.1 Gb/s
Option 200 Range: 50 Mb/s to 14.2 Gb/s	
Option 201 Range: 7.1 Gb/s to 14.2 Gb/s	
Option Bu200: data rate 0.05 to 14.2 Gb/s upgrade	
Option 300: tunable loop bandwidth golden PLL	
Option 100: single-ended and differential electrical with integrated signal taps	
Option 101 Optical Sm: 1260 to 1360 nm and 1490 to 1600 nm, integrated taps	
Option 101 Optical Mm: 830 to 860 nm and 1260 to 1360 nm	
Option 101 Electrical: single-ended or differential electrical inputs (no signal taps) with the optical option	
Specifications	
PARAMETER	VALUE
Host Mainframe	86100C/D (not 86100A/B)
Etr Recommendation	86100D-ETR recommended with 83496x modules
Str Cable	external cable 5062-6690 class from module trigger/clock output to 86100D trigger if Option STR
Form Factor	86100 plug-in
Function	recovered clock for oscilloscope trigger
Predecessor	83496A
Literature	Keysight 86100D DCA configuration guide 5992-0038
Operating Temperature Family	plus 10 C to plus 40 C class of 86100 modules
Application	10 Gb/s-class eyes and jitter with golden PLL
Output	recovered electrical clock
Input	optical SM/MM and/or electrical per option
Firmware	86100C/D required
Notes	
Numeric rate and wavelength rows from Keysight 86100D Infiniium DCA-X configuration guide 5992-0038 (83496B	

option table). Residual jitter of the CDR itself is in the 83496B specification table of the 86100 module data sheet.

Ordering Information

OPTION	DESCRIPTION
Option 200	50 Mb/s to 14.2 Gb/s, Option 201 7.1 to 14.2 Gb/s, Option 300 tunable loop-bandwidth golden PLL, Option 100 electrical taps, and Option 101 SM (1260-1360 and 14
Option 300	adjustable loop BW
Option 201	Range: 7.1 Gb/s to 14.2 Gb/s
Option 101	Optical Sm: 1260 to 1360 nm and 1490 to 1600 nm, integrated taps

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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NIST-traceable calibration · SAM registered ·
30-day returns
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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.