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Data Sheet

August 15, 2026

AGILENT / KEYSIGHT

Agilent/Keysight E4805A

The Keysight E4805A is the central clock and sequencer for the E4859A Serial Cell Generator and Analyzer system. It synthesizes the common system clock from 170 kHz to 660 MHz, synchronizes all E4853A/E4854A modules, and provides trigger outputs for external instruments. Burst-mode TDMA test-system timing, multi-module cell framing, and synchronizing serial cell generators/analyzers in a VXI mainframe. Synthesized system clock for all serial cell modules Internal crystal VXI 10 MHz or external PLL reference Trigger Output Levels: TTL below 180 MHz ECL 50 ohm to GND/-2 V PECL 50 ohm to +3 V Maximum External Voltage Trigger: -2 V to +3 V Operating Temperature System Class: 10 C to 40 C Numeric rows from HP E4859A technical data 5963-9924E E4805A central clock section. Class 001 high frequency resolution is documented as 1 Hz.



MODEL

**Agilent / Keysight
E4805A**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

E4805A

LISTING

<https://aumictechlabs.com/products/e4805a-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Agilent/Keysight E4805A is a central clock module for parallel bit error ratio testing (ParBERT) platforms, engineered to synchronize measurement modules and generate a synthesized system clock for high-speed digital communication verification. Operating as a core component within the E48xxA and 81250 ParBERT ecosystems, it enables precise timing across Mux/Demux, SerDes, and multi-channel transceiver characterization. The module supports clock frequencies from 1

kHz to 660 MHz and accommodates external analyzer clocks recovered from devices under test, making it essential for telecommunications, storage networking, and IC test applications requiring synchronized multi-channel operation.

Technical Specifications

Clock Generation and Input

Central clock frequency range: 1 kHz to 660 MHz Input frequency range: 170 kHz to 250 MHz; 660 MHz with option 660; 330 MHz when DATA IN1 is used in detect-mode Main output bit rates: 170 kbit/s to 250 Mbit/s; optional 660 Mbit/s available Auxiliary outputs disabled above 250 Mbit/s

Analyzer clock: 1 sampling point per bit External analyzer clock: Recovered clock from DUT with minimum eye-opening >400 ps

System Integration

Compatible platforms: Agilent/Keysight E48xxA and 81250 ParBERT Supported data rates: 675 Mb/s to 45 Gb/s (platform dependent)

Internal jitter/wander requirement: Eye-opening >50% of bit period and >1 ns minimum

Pattern Generation

PRBS lengths: $n = 7, 9, 10, 11, 15, 17, 20, 21, 23, 31$ (CCITT O.151); normal or inverted

Memory per channel: 64 Kbit to 1024 Kbit (bit rate dependent)

Pseudo-Random Word Sequences (PRWS) support User-defined and mixed data pattern capability

Maximum frame length: 24 ms with 1 to 16 bit resolution

Guard time: 0 to 24 ms between cells; 10 ps resolution

Cell transfer delay: Manual entry <24 ms with 10 ps granularity

Key Features

Supports multiple transmitter and receiver testing 10 GbE and Forward Error Correction (FEC) device verification Amplifier testing capability Extension for high-speed channels within IC testers

Typical Applications

Serializer/Deserializer (SerDes) characterization Multiplexer/demultiplexer testing Multi-channel transceiver validation High-speed optical and electrical link verification

Compatibility & Integration

Designed exclusively for Agilent/Keysight E48xxA and 81250 ParBERT platforms. Functions as a modular component within larger BERT system architectures, providing centralized clock synchronization across parallel test channels.

E4805A Characteristics / Specifications

PARAMETER	VALUE
Model	E4805A
Instrument Type	central clock and sequencer
Card Format	VXI C-size 1 slot
System Clock Frequency Range	170 kHz to 660 MHz
Frequency Resolution Standard	4 digits
Frequency Resolution With Class 0	1 Hz
Frequency Accuracy Internal PLL	plus or minus 50 ppm
Period Jitter Typical Internal PLL	less than 10 ps rms
PLL Reference Sources	internal crystal VXI bus 10 MHz or external 1 2 5 or 10 MHz
Clock Ref Input Impedance	50 ohm
Clock Ref Input Sensitivity	400 mV
Clock Ref Termination Voltage	-2.10 V to +3.10 V
Clock Ref Input Transitions	less than 20 ns
Clock Ref Input Frequency	170 kHz to 660 MHz
Required Duty Cycle	40 to 60 percent
Clock Ref Connector	SMA female 3.5 mm
Maximum Input Voltage	-3 V to +6 V
Trigger Output Impedance	50 ohm
Trigger Output Levels	TTL below 180 MHz ECL 50 ohm to GND/-2 V PECL 50 ohm to +3 V
Trigger Connector	SMA female 3.5 mm
Maximum External Voltage Trigger	-2 V to +3 V
Operating Temperature System Class	10 C to 40 C
Warm Up Class	30 minutes
Paired Modules	E4853A E4854A
Operating temperature	System Class: 10 C to 40 C

E4805A Specifications

PARAMETER	VALUE
Keysight E4805A Central Clock Module	Overview
Applications	Burst-mode TDMA test-system timing, multi-module cell framing, and synchronizing serial cell generators/analyzers in a VXI mainframe.
Synthesized system clock for all serial cell modules	Internal crystal VXI 10 MHz or external PLL reference
Technical Specifications	Model: E4805A

General Specifications & Supplementary Characteristics

PARAMETER	VALUE
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Paired Modules	E4853A E4854A Notes Numeric rows from HP E4859A technical data 5963-9924E E4805A central clock section. Class 001 high frequency resolution is documented as 1 Hz.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
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Notes

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Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

788 S 500 E, Pleasant Grove, UT 84062
sales@aumictech.com · +1 (484) 841-9341
<https://aumictechlabs.com>

NIST-traceable calibration · SAM registered ·
30-day returns
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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.