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Data Sheet

August 15, 2026

AGILENT / KEYSIGHT

Agilent/Keysight E4838A

Keysight E4838A ParBERT 675 Mb/s Generator Front End The Keysight E4838A is a differential generator front-end for the ParBERT 81250 platform, installing in an E4832A 675 Mb/s data module to stimulate LVDS PECL TTL and CMOS class devices up to 675 Mb/s. Parallel BERT stimulus, Mux/Demux low-speed side generation, and multi-channel digital characterization within ParBERT 81250 clock groups. Single differential generator channel front end The Keysight E4838A is a differential generator front-end for the ParBERT 81250 platform, installing in an E4832A 675 Mb/s data module to stimulate LVDS PECL TTL and CMOS class devices up to 675 Mb/s. Parallel BERT stimulus, Mux/Demux low-speed side generation, and multi-channel digital characterization within ParBERT 81250 clock groups. Single differential generator channel front end Fits one front end slot of E4832A carrier



MODEL

**Agilent / Keysight
E4838A**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

E4838A

LISTING

<https://aumictechlabs.com/products/e4838a-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Agilent/Keysight E4838A is a data generator front-end module for parallel bit error ratio testing in high-speed digital systems. Operating as a plug-in card within the E4832A carrier module, it generates and outputs differential data patterns across a 333 Kb/s to 675 Mb/s range. The module supports pseudo-random word sequences (PRWS), standard PRBS patterns up to $2^{31}-1$, and memory-based patterns up to 2 Mb, with variable transition times between 0.5 and 4.5

ns and typical jitter below 80 ps in data mode. Signal output is configurable between RZ and NRZ formats with amplitudes from 0.1 to 3.5 Vpp, enabling testing of serializer/deserializer (SerDes), multiplexer/demultiplexer architectures, and parallel-to-serial conversion circuits across telecommunications and storage networking applications. Technical Specifications Data Rate Range: 333 Kb/s to 675 Mb/s Output Type: Differential, single channel Output Amplitude: 0.1 to 3.5 Vpp Transition Time (10%-90%): 0.5 to 4.5 ns variable Jitter (Data Mode): <100 ps pp (80 ps typical) Jitter (Clock Mode): 8 ps rms typical Signal Format: RZ/NRZ selectable Pattern Types: PRWS, standard PRBS up to $2^{31}-1$, memory patterns to 2 Mb Weight: 2 lbs Key Features Differential output architecture with selectable RZ/NRZ encoding Fine-grain amplitude control spanning 0.1 to 3.5 Vpp Adjustable edge rates from 0.5 to 4.5 ns transition time Low clock jitter at 8 ps rms typical for precision timing applications Memory-based pattern storage enabling custom test sequences up to 2 Mb Typical Applications Gigabit Ethernet and OC-192 parallel interface testing SerDes and Mux/Demux device characterization Telecom and storage area network (SAN) IC validation 10GbE and forward error correction (FEC) device testing Transmitter and receiver manufacturing test IC-tester high-speed channel extension Compatibility & Integration Requires Keysight Agilent HP E4832A carrier module (one VXI slot) Supports up to four E4838A generator cards per E4832A module Part of Keysight ParBERT 81250 platform End-of-life status: Last order date December 31, 2016

E4838A Characteristics / Specifications

PARAMETER	VALUE
Model	E4838A
Instrument Type	ParBERT 675 Mb/s generator front end
Parent Data Module	E4832A
Channels	1 differential
Impedance Typical	50 ohm
Data Formats	RZ R1 NRZ DNRZ
Output Voltage Window	-2.2 to +4.4 V
Amplitude Range	0.1 V to 3.50 V
Amplitude Resolution	10 mV
Level Accuracy Typical	plus or minus 3 percent plus or minus 25 mV after 5 ns settling
Level Accuracy LVDS PECL Typical	plus or minus 1 percent plus or minus 25 mV after 5 ns settling
Transition Time Range 10 to	0.5 to 4.5 ns
Transition Time Accuracy	plus or minus 5 percent plus or minus 100 ps
Transition Time LVDS PECL Typical 20 to	0.35 ns
Overshoot Ringing	less than 7 percent less than 5 percent typical
Jitter Data Mode	less than 100 ps peak to peak 80 ps typical
Jitter Clock Mode Typical	8 ps rms
Addressable Technologies	LVDS PECL TTL 3.3 V CMOS
Compatible Clocks	E4805B E4808A E4809A
Maximum Channels Per Frame Class	up to 44 at 675 Mb/s
Termination	50 ohm to programmable termination voltage
Differential Termination Selectable	100 ohm
Carrier Slots Occupied	1 front end slot

E4838A Specifications

PARAMETER	VALUE
Keysight E4838A ParBERT 675 Mb/s Generator Front End	Overview
Applications	Parallel BERT stimulus, Mux/Demux low-speed side generation, and multi-channel digital characterization within ParBERT 81250 clock groups.
Single differential generator channel front end	Fits one front end slot of E4832A carrier
RZ R1 NRZ and DNRZ data formats	Variable transition times from 0.5 to 4.5 ns
Technical Specifications	Model: E4838A
Notes	Numeric rows from Agilent ParBERT 81250 datasheet Table 66 E4838A generator front-end section.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
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Instrument Type	ParBERT 675 Mb/s generator front end
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Data Formats	RZ R1 NRZ DNRZ
Output Voltage Window	-2.2 to +4.4 V
Amplitude Range	0.1 V to 3.50 V
Amplitude Resolution	10 mV
Level Accuracy Typical	plus or minus 3 percent plus or minus 25 mV after 5 ns settling
Level Accuracy LVDS PECL Typical	plus or minus 1 percent plus or minus 25 mV after 5 ns settling
Transition Time Range 10 to 90	0.5 to 4.5 ns
Transition Time Accuracy	plus or minus 5 percent plus or minus 100 ps
Transition Time LVDS PECL Typical 20 to 80: 0.35 ns	
Specifications	
PARAMETER	VALUE
Overshoot Ringing	less than 7 percent less than 5 percent typical
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Notes

Numeric rows from Agilent ParBERT 81250 datasheet Table 66 E4838A generator front-end section.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.