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Data Sheet

August 15, 2026

AGILENT / KEYSIGHT

Agilent/Keysight E4861A

Keysight E4861A ParBERT 2.7 Gb/s / 1.65 Gb/s Data Module The Keysight E4861A isaVXI C-size ParBERT 81250 data generator/analyzer module that houses up to two generator or analyzer front-ends. With E4862A/E4863A front-ends the module supports up to 2.7 Gb/s; with E4864A/E4865A front-ends the maximum rate is 1.65 Gb/s. Memory depth reaches 8 Mbit per channel. Mux/Demux and SerDes characterization, parallel and multi-serial BER test, and high-speed digital IC verification on the ParBERT 81250 platform. The Keysight E4861A isaVXI C-size ParBERT 81250 data generator/analyzer module that houses up to two generator or analyzer front-ends. With E4862A/E4863A front-ends the module supports up to 2.7 Gb/s; with E4864A/E4865A front-ends the maximum rate is 1.65 Gb/s. Memory depth reaches 8 Mbit per channel. Mux/Demux and SerDes characterization, parallel and multi-serial BER test, and high-speed digital IC verification on the ParBERT 81250 platform. Two front-end slots for mixed generator/analyzer heads



MODEL Agilent / Keysight E4861A	CALIBRATION Available on request
CONDITION Used	STATUS In stock
RFQ / SKU E4861A	LISTING https://aumictechlabs.com/products/e4861a-2/

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 • 811210 • 541380

This unit

The Agilent/Keysight E4861A is a VXI slot-wide modular component for the ParBERT 81250 Parallel Bit Error Ratio Tester platform, enabling high-speed parallel stimulus generation and analysis. It accommodates two front-end plug-in cards for generator and analyzer functions, supporting data rates from 333 Mb/s to 2.7 Gb/s and testing of multi-channel devices including

multiplexers, demultiplexers, and SerDes circuits up to 40G. Technical Specifications Data Rate and Operating Range Data rates: 333 Mb/s to 2.7 Gb/s (E4862A/E4863A front-ends) or 333 Mb/s to 1.65 Gb/s (E4864A/E4865A front-ends) ParBERT 81250 system range: 675 Mb/s to 45 Gb/s (across various modules) Pattern generation: PRBS up to $2^{31}-1$, pseudo-random word sequences (PRWS), user-defined patterns up to 64 Mb Generator Front-End (E4862A/E4864A) Output amplitude: 0.5 Vpp to 1.8 Vpp variable Transition time (20%–80%): 90 ps typical Data mode jitter: <50 ps peak-to-peak Clock mode jitter: <5 ps RMS Operates in clock mode (50% duty cycle, Pulse Port) or NRZ data mode with variable delay (Data Port) Analyzer Front-End (E4863A/E4865A) Input impedance: 50 Ω Input sensitivity: 50 mV Input voltage range: –2 V to +3 V Key Features Dual front-end capacity per module for flexible configuration Supports differential and single-ended signal interfaces Integrated bit error ratio (BER) analysis with multiple pattern modes Automatic synchronization and alignment capability Modular architecture for scalable parallel testing Typical Applications Parallel-side testing of multiplexer/demultiplexer and SerDes devices High-speed telecommunications IC validation (e.g., OC-768) Storage area network component characterization Multi-channel digital communication device verification Compatibility & Integration The E4861A integrates within the ParBERT 81250 ecosystem, supporting mixed module configurations for data rates spanning 675 Mb/s to 45 Gb/s across the platform.

E4861A Characteristics / Specifications

PARAMETER	VALUE
Model	E4861A
Instrument Type	ParBERT 81250 data generator analyzer module
Card Format	VXI C-size 1 slot
Front End Slots	2
Max Data Rate With E4862A E4863A	2.7 Gb/s
Max Data Rate With E4864A E4865A	1.65 Gb/s
Data Rate Range Clock Data Mode	333.334 Mb/s to 2.70 Gb/s
Memory Depth Per Channel	up to 8 Mbit
PRBS PRWS Polynomials	$2^n - 1$ n equals 7 9 10 11 15 23 31
Mark Density Settings	1/8 1/4 1/2 3/4 7/8 for n equals 7 9 10 11 15
Generator Delay Range	0 to 300 ns
Generator Delay Resolution	1 ps
Generator Delay Accuracy	plus or minus 50 ps plus or minus 50 ppm relative to zero delay
Skew Between Modules Typical	50 ps after deskew
Max Memory At 64 Bit Segment Resolution	8388608 bits
Segment Length At 333.334 To 666.666 Mb/s	16 bits resolution 2097152 bits max
Segment Length At 666.667 To 1333.333 Mb/s	32 bits resolution 4194304 bits max
Segment Length At 1333.334 To 2666.667 Mb/s	64 bits resolution 8388608 bits max
Compatible Clock Modules	E4805B E4808A
Channels Per Module	up to 2
Channels Per Frame Class	up to 22 at 2.7 Gb/s class
Module Mass Net Typical	2 kg including front-ends
Programming Interface	GPIB IEEE 488.2 and LAN

PARAMETER	VALUE
Data Rate	With E4862A E4863A: 2.7 Gb/s

E4861A Specifications

PARAMETER	VALUE
Keysight E4861A ParBERT 2.7 Gb/s / 1.65 Gb/s Data Module	Overview
Compatible with E4805B and E4808A central clock modules	Differential and single-ended CML PECL ECL LVDS SSTL-2 class I/O via front-ends
Technical Specifications	Model: E4861A

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
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Notes	
Numeric rows from Agilent ParBERT 81250 Parallel Bit Error Ratio Tester datasheet 5968-9188E. Front-end	

amplitude timing and technology limits are stated on the matched E4862A/E4863A or E4864A/E4865A sheets.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.