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Data Sheet

August 15, 2026

AGILENT / KEYSIGHT

Agilent/Keysight M8041A

Keysight M8041A J-BERT Pattern Generator Module The Keysight M8041A is the J-BERT M8020A pattern generator module providing calibrated stressed serial outputs with integrated jitter and de-emphasis for receiver characterization up to 8.5 or 16.2 Gb/s depending on installed rate options. Multi-lane receiver stress testing, compliance pattern generation, and aggressor lane emulation within M8020A AXIe BERT systems. Integrated into M8020A multi-channel BERT architecture The Keysight M8041A is the J-BERT M8020A pattern generator module providing calibrated stressed serial outputs with integrated jitter and de-emphasis for receiver characterization up to 8.5 or 16.2 Gb/s depending on installed rate options. Multi-lane receiver stress testing, compliance pattern generation, and aggressor lane emulation within M8020A AXIe BERT systems. Integrated into M8020A multi-channel BERT architecture Calibrated jitter sources when advanced jitter option present



MODEL

**Agilent / Keysight
M8041A**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

M8041A

LISTING

<https://aumictechlabs.com/products/m8041a-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 • 811210 • 541380

This unit

The Keysight M8041A is a J-BERT module engineered for receiver characterization and link validation across single and multi-lane high-speed digital interfaces. Operating within the M8020A BERT system architecture, it delivers pattern generation and error detection to 8.5 Gb/s and 16 Gb/s, supporting up to four 16 Gb/s BERT channels in a 3-slot AXIe chassis with expansion

capability to 32 Gb/s via the M8061A multiplexer or M8062A front-end. The module excels at jitter injection and characterization. It integrates calibrated sources for Random Jitter (RJ), Periodic Jitter (PJ1, PJ2), Spurious Jitter (SJ), Bursty Jitter (BUJ), sinusoidal interference in common-mode and differential-mode configurations, and Spread Spectrum Clocking (SSC) in triangular, arbitrary, and residual variants. An 8-tap de-emphasis stage (positive and negative) provides up to 20 dB of adjustment, while integrated and adjustable Intersymbol Interference (ISI) emulates channel loss effects. Link training capabilities span PCI Express at 8 GT/s and 16 GT/s, SAS-3, and USB 3.0/3.1 protocols. The module supports interactive TxEQ training for IEEE 10GBASE-KR, 25GBASE-KR, and 100GBASE-KR4 applications. Built-in clock data recovery (CDR) and equalization streamline test configurations; analyzer equalization is available as an option (M8041A-0A3).

Technical Specifications

Data Rates: 8.5 Gb/s and 16 Gb/s pattern generator and error detector BERT

Channels: Up to four 16 Gb/s channels per 3-slot AXIe chassis; expandable to 32 Gb/s

De-emphasis: 8-tap topology, $\pm$ polarity, up to 20 dB adjustment range

Reference Clock Input: 0.2 to 1.4 V_{pp} amplitude; 10 MHz to 16.2 GHz (or 16.5 GHz) frequency; 50 Ω single-ended; SMA female connector

Control I/O: Four universal control inputs with adjustable threshold; three universal control outputs with adjustable levels

Key Features

Jitter injection: RJ, PJ1/PJ2, SJ, BUJ, sinusoidal (CM/DM), SSC (triangular/arbitrary/residual)

Adjustable ISI for loss emulation

Interactive link training: PCIe, SAS-3, USB 3.0/3.1, and IEEE KR protocols

Built-in CDR and equalization

Typical Applications

High-speed serial interface receiver characterization

Protocol compliance and link training validation

Jitter tolerance and channel loss testing

Multi-lane device verification

Compatibility & Integration

Designed for 3-slot AXIe chassis integration. Expansion to 32 Gb/s via M8061A multiplexer or M8062A BERT front-end.

M8041A Characteristics / Specifications

PARAMETER	VALUE
Model	M8041A
Instrument Type	J-BERT pattern generator module
Parent System	M8020A
Data Rate Option G08/C	256 Mb/s to 8.50 Gb/s
Data Rate Option G16/C	256 Mb/s to 16.20 Gb/s
Intrinsic Total Jitter Typical	8 ps peak to peak at 0.5 V into ground
Intrinsic Random Jitter Typical	300 fs rms
Data Delay Range	0 to 10 ns
Data Delay Resolution	100 fs
Crossing Point Adjust	30 percent to 70 percent
Transition Time Fast Typical	12 ps 20 to 80 percent
Transition Time Moderate Typical	17 ps 20 to 80 percent
Transition Time Smooth Typical	20 ps 20 to 80 percent
De Emphasis Taps	8
Form Factor	AXIe module for M8020A chassis
Output Measurement Reference	0.5 V into ground timing specs
PRBS Polynomial Support Class	standard J-BERT PRBS set including 2^n-1 family
Electrical Idle	supported with fast amplitude collapse to idle
Clock Modes	internal and reference locked class
Channel Role	pattern generator within multi-lane BERT
Data Rate	Option G08/C08: 256 Mb/s to 8.50 Gb/s

M8041A Specifications

PARAMETER	VALUE
Applications	Multi-lane receiver stress testing, compliance pattern generation, and aggressor lane emulation within M8020A AXIe BERT systems.
Key Features	Integrated into M8020A multi-channel BERT architecture
Technical Specifications	Model: M8041A
Notes	Numeric rows from Keysight J-BERT M8020A data sheet M8041A generator timing table.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
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Notes	
Numeric rows from Keysight J-BERT M8020A data sheet M8041A generator timing table.	

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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NIST-traceable calibration · SAM registered ·
30-day returns
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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.