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Data Sheet

August 14, 2026

AGILENT / KEYSIGHT

Agilent/Keysight N4903B

Agilent Keysight N4903B J-BERT High-Performance Serial BERT 7 12.5 14.2 Gb/s The Keysight J-BERT N4903B is the flagship N4900 serial BERT for characterization to 14.2 Gb/s (28.4 Gb/s with external 2:1 mux/demux and CDR). OEM N4903B data sheet 5990-3217 lists 150 Mb/s to 7, 12.5, or 14.2 Gb/s; intrinsic jitter 800 fs rms; transition times less than 20 ps; always-included tunable CDR; and calibrated SJ, PJ, SSC, RJ, BUJ, and ISI. USB 3.1, PCIe, SATA, SAS, 10/40/100GbE, and optical-transceiver receiver jitter-tolerance and BER. The Keysight J-BERT N4903B is the flagship N4900 serial BERT for characterization to 14.2 Gb/s (28.4 Gb/s with external 2:1 mux/demux and CDR). OEM N4903B data sheet 5990-3217 lists 150 Mb/s to 7, 12.5, or 14.2 Gb/s; intrinsic jitter 800 fs rms; transition times less than 20 ps; always-included tunable CDR; and calibrated SJ, PJ, SSC, RJ, BUJ, and ISI. USB 3.1, PCIe, SATA, SAS, 10/40/100GbE, and optical-transceiver receiver jitter-tolerance and BER. Option D14 pattern-generator extension to 14.2 Gb/s



MODEL

**Agilent / Keysight
N4903B**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

N4903B

LISTING

<https://aumictechlabs.com/products/n4903b-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Keysight N4903B is a multi-channel serial Bit Error Rate Tester (BERT) designed for R&D and validation of high-speed digital communication systems. It delivers precise characterization and stress testing of transceiver modules and devices with serial I/O ports across industry-standard

interfaces. The instrument combines pattern generation, error detection, and integrated jitter injection to validate receiver tolerance and transmitter performance in advanced digital interfaces. Technical Specifications Data Rate Performance Pattern Generator and Error Detector: 150 Mb/s to 7 Gb/s, or up to 12.5 Gb/s Extended capability with option: 14.2 Gb/s Maximum with 2:1 multiplexer and demultiplexer: 28.4 Gb/s Jitter Injection and Measurement Integrated, calibrated jitter sources exceeding 0.5 UI Random Jitter (RJ): 0 to 20 mUI rms (0 to 280 mUI pp) Periodic Jitter (PJ1 + PJ2) with Option D14 (>12.5 Gb/s): 0 to 2.0 UI Jitter modulation frequency: 1 kHz to 100 MHz Jitter types: RJ, RJ-LF, RJ-HF, PJ1, PJ2, Sine Jitter, Bursty Jitter, Inter-Symbol Interference, sinusoidal interference, triangular and arbitrary Spread Spectrum Clocking, residual SSC Clock and Data Recovery Built-in CDR with tunable, compliant loop bandwidth Half-rate clocking with variable duty cycle (Option 003) Operation at full or half bit-rate Pattern Generation PRBS and user-defined patterns 60-block pattern sequencer with real-time switching via auxiliary input Independent PRBS and pattern generation on auxiliary data output Key Features Bit Error Rate, BER Contour, and automated jitter tolerance measurements Total Jitter with RJ/DJ separation and Eye Diagram analysis Eye Mask testing and Frame Error Rate (FER) detection Symbol Error Rate (SER) on coded and retimed data streams Pattern Capture functionality Differential I/Os optimized for serial bus standards Typical Applications Receiver jitter tolerance characterization Transmitter signal quality validation Serial I/O compliance testing Device stress testing and margin analysis Compatibility & Integration Differential I/O interfaces designed to match serial bus standards. Supports Option 003 for half-rate clocking and duty cycle distortion testing.

N4903B Characteristics / Specifications

PARAMETER	VALUE
Instrument Type	High-performance serial BERT (J-BERT)
Series Family	Keysight N4900 J-BERT
Data Rate Option D	150 Mb/s to 14.2 Gb/s (requires C13 or G13)
Data Rate Option C	150 Mb/s to 12.5 Gb/s, programmable to 13.5 Gb/s
Mux Extension	28.4 Gb/s with 2:1 multiplexer/demultiplexer and CDR
Intrinsic Jitter	800 fs rms
Transition Time	less than 20 ps
Pattern Sequencer	up to 120 blocks with counted loops
Clock Data Recovery	built-in tunable CDR always included
Remote Interfaces	LAN, USB, and GPIB
Delay Lines For Jitter Sweep	610 ps or 220 ps delay line for automated JTOL
Literature	Keysight J-BERT N4903B data sheet 5990-3217
Data Rate	Option D14: 150 Mb/s to 14.2 Gb/s (requires C13 or G13)

N4903B Specifications

PARAMETER	VALUE
Applications	USB 3.1, PCIe, SATA, SAS, 10/40/100GbE, and optical-transceiver receiver jitter-tolerance and BER.
Electrical idle on data outputs	8b/10b and 128b/130b coded-data error analysis with SKP OS filtering
Technical Specifications	Instrument Type: High-performance serial BERT (J-BERT)

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Performance Serial BERT 7 12.5 14.2 Gb/s

Overview

The Keysight J-BERT N4903B is the flagship N4900 serial BERT for characterization to 14.2 Gb/s (28.4 Gb/s with external 2:1 mux/demux and CDR). OEM N4903B data sheet 5990-3217 lists 150 Mb/s to 7, 12.5, or 14.2 Gb/s; intrinsic jitter 800 fs rms; transition times less than 20 ps; always-included tunable CDR; and calibrated SJ, PJ, SSC, RJ, BUJ, and ISI.

Applications

USB 3.1, PCIe, SATA, SAS, 10/40/100GbE, and optical-transceiver receiver jitter-tolerance and BER.

Key Features

Always-included tunable CDR

Option D14 pattern-generator extension to 14.2 Gb/s

Second output channel with independent pattern/PRBS (Option 002)

Electrical idle on data outputs

8b/10b and 128b/130b coded-data error analysis with SKP OS filtering

Technical Specifications

Technical Specifications

PARAMETER	VALUE
Instrument Type	High-performance serial BERT (J-BERT)
Series Family	Keysight N4900 J-BERT
Data Rate Option D14	150 Mb/s to 14.2 Gb/s (requires C13 or G13)
Data Rate Option C13	150 Mb/s to 12.5 Gb/s, programmable to 13.5 Gb/s
Data Rate Option C07	150 Mb/s to 7 Gb/s
Mux Extension	28.4 Gb/s with 2:1 multiplexer/demultiplexer and CDR
Intrinsic Jitter	800 fs rms
Transition Time	less than 20 ps
Pattern Sequencer	up to 120 blocks with counted loops
Clock Data Recovery	built-in tunable CDR always included

Option G07 G13: pattern generator without error detector at 7 or 12.5 Gb/s

Option 002: PRBS and pattern on aux data output (second channel)

Option 003: half-rate clock with variable duty cycle

Option J10: RJ, sRJ, PJ1, PJ2, SJ, BUJ injection

Option J11: SSC and residual SSC generation

Option J20: interference channel (includes N4915A-008 short cable kit)

Option J12: jitter tolerance compliance suite

Option A01: bit recovery mode

Option A02: SER/FER analysis

Option UAB: factory upgrade from N4903A

Specifications

PARAMETER	VALUE
Remote Interfaces	LAN, USB, and GPIB
Delay Lines For Jitter Sweep	610 ps or 220 ps delay line for automated JTOL
Literature	Keysight J-BERT N4903B data sheet 5990-3217

Notes

Numeric rows from Keysight J-BERT N4903B High-Performance Serial BERT data sheet 5990-3217 (rates C07/C13/D14, 800 fs rms, less than 20 ps, 120-block sequencer, option codes). Remove the CDR loop-bandwidth row if not on the N4903B table; tunable CDR is always included per that data sheet. Full amplitude/sensitivity tables are in the specification chapter.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.