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Data Sheet

August 14, 2026

AGILENT / KEYSIGHT

Agilent/Keysight P5551A

Agilent Keysight P5551A PCI Express 5.0 Protocol Exerciser The Keysight P5551A isaPCIe 5.0 protocol exerciser used with the P5552A analyzer to emulate root complexes and endpoints. OEM P5551A/P5552A data sheets list link widths x1 through x16, data rates 2.5/5.0/8.0/16.0/32 GT/s (Gen1-Gen5), 32 GBaud NRZ per lane, common-clock architecture, and a standard-height half-length PCIe module 106.7 mm high by 167.65 mm long weighing 408 g. PCIe 5.0 endpoint and root-complex validation, LTSSM bring-up, and paired analyzer traffic generation on the lab bench. The Keysight P5551A isaPCIe 5.0 protocol exerciser used with the P5552A analyzer to emulate root complexes and endpoints. OEM P5551A/P5552A data sheets list link widths x1 through x16, data rates 2.5/5.0/8.0/16.0/32 GT/s (Gen1-Gen5), 32 GBaud NRZ per lane, common-clock architecture, and a standard-height half-length PCIe module 106.7 mm high by 167.65 mm long weighing 408 g. PCIe 5.0 endpoint and root-complex validation, LTSSM bring-up, and paired analyzer traffic generation on the lab bench. Link widths x4/x8/x16 order codes E04/E08/E16



MODEL

**Agilent / Keysight
P5551A**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

P5551A

LISTING

<https://aumictechlabs.com/products/p5551a-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Agilent/Keysight P5551A is a PCIe 5.0 Protocol Exerciser for testing and validating PCIe designs across all major protocol generations. It emulates both PCIe root complex and endpoint devices, enabling comprehensive verification and debug of PCIe implementations. The instrument

supports PCIe 1.0 through 5.0 standards with data rates from 2.5 GT/s (Gen1) to 32 GT/s (Gen5), accommodating lane widths of x4, x8, and x16. Technical Specifications Protocol Support PCIe 1.0, 2.0, 3.0, 4.0, and 5.0 standards Data rates: 2.5 GT/s to 32 GT/s Lane configurations: x4, x8, x16 Automated link training to 32 GT/s Speed change capability from 2.5 GT/s to maximum supported speed PCIe 5.0 link training bypass support Electrical Characteristics Follows all PCIe 5.0 electrical specifications Trigger Output: 50 Ω impedance, VOH 2.4 V, VOL 0.55 V, 2.4 V amplitude (open), 1.2 V amplitude (50 Ω load), 120 nS pulse width Trigger Input: Maximum 3.0 V, VIH 2.0 V Environmental Operating temperature: +5 °C to +35 °C Installation category II, pollution degree 2 (indoor use) Key Features Single add-in-card design with improved signal integrity Configurable signal integrity characteristics for variable test environments Precise power management stimulus for L0, L0s, and L1 substates Integrated low-noise power supply with auxiliary PCIe power for high-power endpoints Over 100 built-in LTSSM test cases LTSSM state machine control and support (all states except L2 and Loopback) Lane reversal and polarity detection Scalable flow control support Traffic generation via GUI or automated scripts (C# and Python APIs) Interfaces and Connectors Power input connector USB 3.0 Two SMA(f) connectors (trigger in/out) PCIe edge connector (width configurable per lane width) Typical Applications Root complex and endpoint device emulation for PCIe design validation Link training and protocol compliance testing Power state management verification Signal integrity characterization and optimization LTSSM behavior validation across PCIe generations

P5551A Characteristics / Specifications

PARAMETER	VALUE
Instrument Type	PCI Express 5.0 protocol exerciser
Series Family	Keysight P5500 PCIe protocol test
Link Widths	x1, x2, x4, x8, x16
Data Rates	2.5 GT/s Gen1, 5.0 GT/s Gen2, 8.0 GT/s Gen3, 16.0 GT/s Gen4, 32 GT/s Gen5
Lane Speed	32 GBaud NRZ per lane
Clocking Architecture	common clock
Module Size	standard-height half-length PCIe; 106.7 mm (4.2 in) high and 167.65 mm (6.6 in) long
Weight	408 g (0.9 lb); shipping weight 2.36 kg (5.2 lb)
External Supply	Keysight 0950-6474; 100 to 240 V at 4.0 A maximum, 50 to 60 Hz
Order E	PCIe 5.0 exerciser link width x16
Required Software	P5551PSWA PCIe 5.0 exerciser software
Companion Analyzer	P5552A
Companion Backplane	P5563A PCIe 5.0 test system
Card Holder	P5500A
Literature	Keysight P5551A PCI Express Protocol Exerciser data sheet
Use With Analyzer	paired P5551A plus P5552A validation solution
Package Form	PCIe add-in card exerciser (notachassis analyzer)
Protocol Generations	PCIe 1.0 through 5.0
Host Connector Class	x16 PCIe edge finger
Software App	P5500 Protocol Testing application family

P5551A Specifications

PARAMETER	VALUE
Applications	PCIe 5.0 endpoint and root-complex validation, LTSSM bring-up, and paired analyzer traffic generation on the lab bench.
Emulates PCIe root complex or endpoint	Gen1 through Gen5 rates to 32 GT/s
Link widths x4/x8/x16 order codes E04/E08/E16	Pairs with P5552A analyzer and P5563A backplane
Technical Specifications	Instrument Type: PCI Express 5.0 protocol exerciser

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
Specifications	
PARAMETER	VALUE
Instrument Type	PCI Express 5.0 protocol exerciser
Series Family	Keysight P5500 PCIe protocol test
Link Widths	x1, x2, x4, x8, x16
Data Rates	2.5 GT/s Gen1, 5.0 GT/s Gen2, 8.0 GT/s Gen3, 16.0 GT/s Gen4, 32 GT/s Gen5
Lane Speed	32 GBaud NRZ per lane
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Module Size	standard-height half-length PCIe; 106.7 mm (4.2 in) high and 167.65 mm (6.6 in) long
Weight	408 g (0.9 lb); shipping weight 2.36 kg (5.2 lb)
External Supply	Keysight 0950-6474; 100 to 240 V at 4.0 A maximum, 50 to 60 Hz
Order E04	PCIe 5.0 exerciser link width x4
Order E08	PCIe 5.0 exerciser link width x8
Order E16	PCIe 5.0 exerciser link width x16
Required Software	P5551PSWA PCIe 5.0 exerciser software
Companion Analyzer	P5552A
Companion Backplane	P5563A PCIe 5.0 test system
Card Holder	P5500A
Literature	Keysight P5551A PCI Express Protocol Exerciser data sheet
Use With Analyzer	paired P5551A plus P5552A validation solution
Package Form	PCIe add-in card exerciser (notachassis analyzer)
Protocol Generations	PCIe 1.0 through 5.0
Host Connector Class	x16 PCIe edge finger
Software App	P5500 Protocol Testing application family
Notes	
Link rates, widths, size, weight, and PSU 0950-6474 from Keysight P5551A PCI Express Protocol Exerciser product specifications. Analyzer-side 16 GB trace memory is on P5552A, not this exerciser.	

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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NIST-traceable calibration · SAM registered ·
30-day returns
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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.