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Data Sheet

August 14, 2026

AGILENT / KEYSIGHT

Agilent/Keysight P5552A

Agilent Keysight P5552A PCI Express 5.0 Protocol Analyzer The Keysight P5552A isaPCIe 5.0 protocol analyzer with an integrated interposer (no separate analyzer chassis). OEM data sheet and hardware guide list capture/decode for PCIe 1.0 through 5.0, 32 GT/s, lane widths x4/x8/x16 (x16 edge connector), 16 GB trace memory with on-board compression, PHY/Link/Transaction decode, USB 3.0 plus SMA trigger I/O, and 12 Vdc at 18 A (230 W max). In-band PCIe 5.0 interoperability debug between host and endpoint with minimal channel impact, optionally paired with the P5551A exerciser. The Keysight P5552A isaPCIe 5.0 protocol analyzer with an integrated interposer (no separate analyzer chassis). OEM data sheet and hardware guide list capture/decode for PCIe 1.0 through 5.0, 32 GT/s, lane widths x4/x8/x16 (x16 edge connector), 16 GB trace memory with on-board compression, PHY/Link/Transaction decode, USB 3.0 plus SMA trigger I/O, and 12 Vdc at 18 A (230 W max). In-band PCIe 5.0 interoperability debug between host and endpoint with minimal channel impact, optionally paired with the P5551A exerciser.

**MODEL****Agilent / Keysight
P5552A****CALIBRATION****Available on
request****CONDITION****Used****STATUS****In stock****RFQ / SKU****P5552A****LISTING**<https://aumictechlabs.com/products/p5552a-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Agilent/Keysight P5552A is a PCIe 5.0 Protocol Analyzer that captures and decodes protocol traffic across PCIe 1.0 through PCIe 5.0 systems. Built as an integrated interposer card, it installs directly into a PCIe slot without requiring external chassis infrastructure, minimizing signal

integrity degradation and simplifying lab integration. The analyzer supports data rates to 32 GT/s across x4, x8, and x16 lane configurations, with 16 GB of on-board trace memory and hardware-based data compression for extended capture sessions.

Technical Specifications

Data Rate: PCIe 1.0 through PCIe 5.0, up to 32 GT/s

Lane Configuration: x4, x8, x16 physical lane widths

Trace Memory: 16 GB with on-board data compression

Protocol Coverage: PHY layer (TS1/TS2/Ordered sets), Link layer (ACK/NAL, Sequencing Numbers, Replay), Transaction layer (Memory, Config, I/O read/writes)

Power Input: 12 Vdc, 18 A maximum; 230 W maximum power requirement

Trigger Output: 50 ohm impedance; VOH 2.4 V, VOL 0.55 V

Trigger Input: 3.0 V maximum; VIH 2.0 V

Key Features

- Integrated equalization and amplification for signal integrity control
- Advanced trigger and filter engine with If/Then logic configuration for complex protocol event capture
- PCIe Gen6 x16 edge finger with 164 gold-plated pins (82 top, 82 bottom)
- Bracket mount and optional stability bracket for secure installation
- Independent power supply passes host power to endpoint without interference
- Hardware cover for mechanical rigidity

Interfaces

- One USB 3.0 female port
- Two SMA(f) connectors (trigger in and out)

Compatibility & Integration

- Operates with P5552PSWA Protocol Analyzer Traffic Analysis Software
- Supports PCIe 1.0, 2.0, 3.0, 4.0, and 5.0 standards
- Compatible with Keysight P5551A Protocol Exerciser for paired testing workflows

P5552A Characteristics / Specifications

PARAMETER	VALUE
Instrument Type	PCI Express 5.0 protocol analyzer with integrated interposer
Series Family	Keysight P5500 PCIe protocol test
Link Widths	x1, x2, x4, x8, x16 with x16 PCIe edge connector
Data Rates	2.5 GT/s Gen1, 5.0 GT/s Gen2, 8.0 GT/s Gen3, 16.0 GT/s Gen4, 32 GT/s Gen5
Lane Speed	32 GBaud NRZ per lane
Clocking Architecture	common clock
Trace Memory	16 GB with on-board compression
Protocol Layers	PHY (TS1/TS2/ordered sets), Link (ACK/NAK, sequence, replay), Transaction (memory, config, I/O)
Dimensions	167.65 mm long, 235.0 mm high, 20.0 mm wide (hardware guide); data sheet also states 235 mm high and 167 mm long
Weight Hardware Guide	0.9 kg
Weight Data Sheet	less than 1.5 kg
Connectors	power input, USB 3.0, two SMA(f) trigger in and out
Dc Input	12 Vdc, 18 A maximum
Maximum Power	230 W
Edge Finger	PCIe x16, 82 gold pins top and 82 bottom (164 pins)
Trigger Input Low	0 V min, 0.9 V max
Trigger Input High	2.0 V min, 3.3 V max
Trigger Input Current	plus or minus 5 uA
Trigger Input Impedance	50 ohm
Trigger Threshold	2.0 V, falling edge
Operating Temperature	plus 5 C to plus 35 C
Storage Temperature	minus 40 C to plus 70 C
Operating Humidity	15 to 85 percent RH
Storage Humidity	15 to 95 percent RH

PARAMETER	VALUE
Altitude	2000 m (6500 ft) maximum
Safety	IEC 61010-1 / EN 61010-1; CSA C22.2 No. 61010-1; UL 61010-1
Emc	IEC 61326-1
Order A04 A08 A	analyzer link width x4 / x8 / x16
Required Software	P5552PSWA PCIe 5.0 analyzer software
Literature	Keysight P5552A PCI Express Protocol Analyzer data sheet 3122-1321 and hardware guide
Humidity	15 to 85 percent RH

General Specifications & Supplementary Characteristics

PARAMETER	VALUE
Storage temperature	minus 40 C to plus 70 C
Operating temperature	plus 5 C to plus 35 C
Operating Temperature	plus 5 C to plus 35 C
Humidity	15 to 85 percent RH
Operating Humidity	15 to 85 percent RH
Storage Humidity	15 to 95 percent RH
Altitude	2000 m (6500 ft) maximum
Safety	IEC 61010-1 / EN 61010-1; CSA C22.2 No. 61010-1; UL 61010-1
Emc	IEC 61326-1
Order A04 A08 A	analyzer link width x4 / x8 / x16
Required Software	P5552PSWA PCIe 5.0 analyzer software
Literature	Keysight P5552A PCI Express Protocol Analyzer data sheet 3122-1321 and hardware guide Notes Rates, memory, power, size, and trigger I/O from Keysight P5552A PCI Express Protocol Analyzer data sheet 3122-1321 and P5552 PCIe Gen5 Analyzer Hardware Guide.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
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Data Rates	2.5 GT/s Gen1, 5.0 GT/s Gen2, 8.0 GT/s Gen3, 16.0 GT/s Gen4, 32 GT/s Gen5
Lane Speed	32 GBaud NRZ per lane
Clocking Architecture	common clock
Trace Memory	16 GB with on-board compression
Protocol Layers	PHY (TS1/TS2/ordered sets), Link (ACK/NAK, sequence, replay), Transaction (memory, config, I/O)
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Emc	IEC 61326-1
Order A04 A08 A16	analyzer link width x4 / x8 / x16
Required Software	P5552PSWA PCIe 5.0 analyzer software
Literature	Keysight P5552A PCI Express Protocol Analyzer data sheet 3122-1321 and hardware guide

Notes
Rates, memory, power, size, and trigger I/O from Keysight P5552A PCI Express Protocol Analyzer data sheet 3122-1321 and P5552 PCIe Gen5 Analyzer Hardware Guide.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

788 S 500 E, Pleasant Grove, UT 84062
sales@aumictech.com · +1 (484) 841-9341
<https://aumictechlabs.com>

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.