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Data Sheet

August 15, 2026

AGILENT / KEYSIGHT

Agilent/Keysight U4305B

Keysight U4305B Protocol Exerciser for PCI Express 3.0 The Keysight U4305B is a standard-height half-length PCIe Gen3 protocol exerciser card that emulates root complex or endpoint behavior for thorough link, LTSSM, power management, and optional NVMe/SR-IOV validation. PCIe Gen1/2/3 bring-up, LTSSM state coverage, L1 substate power validation, NVMe conformance, and scripted traffic generation in servers and blade systems. Emulates root complex or add in card roles The Keysight U4305B is a standard-height half-length PCIe Gen3 protocol exerciser card that emulates root complex or endpoint behavior for thorough link, LTSSM, power management, and optional NVMe/SR-IOV validation. PCIe Gen1/2/3 bring-up, LTSSM state coverage, L1 substate power validation, NVMe conformance, and scripted traffic generation in servers and blade systems. Emulates root complex or add in card roles

Instrument Type: PCIe 3.0 protocol exerciser



MODEL

**Agilent / Keysight
U4305B**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

U4305B

LISTING

<https://aumictechlabs.com/products/u4305b-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Keysight U4305B is a PCIe protocol exerciser module that validates and debugs PCI Express devices and systems across Gen1, Gen2, and Gen3 speeds. Operating as either a root complex or endpoint emulator, it generates and responds to transaction layer packets, data link layer packets, and physical layer traffic. The module supports link widths from x1 to x16 and includes advanced

capabilities for NVMe emulation, power management testing, LTSSM validation, and PCI-SIG compliance testing. Error injection, protocol checking, and data replay from captured analyzer sessions enable thorough device characterization. Control is provided via graphical user interface or APIs supporting TCL, Python, C++, and C# for automated test development and execution. Technical Specifications PCIe Gen1 (2.5 GT/s), Gen2 (5.0 GT/s), and Gen3 (8.0 GT/s) operation Link widths: x1, x2, x4, x8, x16 Emulates up to three device functions (standard), expandable to five (optional) NVMe host root complex emulation with scripting support Optional MR-IOV and SR-IOV emulation Power dissipation: 70 W max AC input: 100–240 V at 3.5 A max, 50–60 Hz Form factor: Standard height, half-length card No external memory module required Key Features Advanced traffic generator for TLP (32-bit and 64-bit memory, I/O, Configuration, Message types), DLLP, and physical layer packets LTSSM testing with detailed failure reporting PCI-SIG compliance test (PTC) execution Power state testing: L0s, L1, and L1 substates Error insertion: CRC errors, bit errors, poison TLP Protocol checker and DUT configuration space exploration Data replay from U4301A/B PCIe analyzer captures Protocol exerciser GUI and multi-language API control API logging for test case automation Typical Applications PCIe device validation across multiple generations NVMe controller and host root complex emulation Link training and power management validation Compliance testing and error injection analysis Compatibility & Integration Software installation: Client and Full setup types Minimum 256 MB RAM (512 MB or higher recommended) Host processor: Pentium 1 GHz or equivalent Supported programming languages: TCL, Python, C++, C#

U4305B Characteristics / Specifications

PARAMETER	VALUE
Model	U4305B
Instrument Type	PCIe 3.0 protocol exerciser
Form Factor	standard height half length PCIe card
Line Rate Gen	2.5 GT/s
Link Widths	x1 ×2 ×4 ×8 ×16
Emulated Roles	root complex and endpoint
Operating Modes	PCIe MR IOV SR IOV
Standard Emulated Functions	3
Traffic Layers Stimulated	TLP DLLP physical layer ordered sets
Error Injection Class	CRC bit errors poison TLP
Power Management Tests	L0s L1 and L1 substates
Sideband Clock Request	CLKREQ support for L1 substates
Analyzer Replay Source Class	U4301A/B captured traffic
NVMe Emulation	optional root complex and endpoint
Equalization Control	transceiver equalization controls
Control Interfaces	GUI and DCOM API
DC Supply Class External Adapter	15 V 10 A max 70 W class

U4305B Specifications

PARAMETER	VALUE
Keysight U4305B Protocol Exerciser for PCI Express 3.0	Overview
Emulates root complex or add in card roles	Supports Gen1 Gen2 and Gen3 line rates
Technical Specifications	Model: U4305B
Notes	Numeric rows from Keysight U4305B Protocol Exerciser for PCI Express 3.0 data sheet and product literature.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
Specifications	
PARAMETER	VALUE
Model	U4305B
Instrument Type	PCIe 3.0 protocol exerciser
Form Factor	standard height half length PCIe card
Line Rate Gen1	2.5 GT/s
Line Rate Gen2	5.0 GT/s
Line Rate Gen3	8.0 GT/s
Link Widths	x1 x2 x4 x8 x16
Emulated Roles	root complex and endpoint
Operating Modes	PCIe MR IOV SR IOV
Standard Emulated Functions	3
Optional Emulated Functions: up to 5	
Specifications	
PARAMETER	VALUE
Traffic Layers Stimulated	TLP DLLP physical layer ordered sets
Error Injection Class	CRC bit errors poison TLP
Power Management Tests	L0s L1 and L1 substates
Sideband Clock Request	CLKREQ support for L1 substates
Analyzer Replay Source Class	U4301A/B captured traffic
NVMe Emulation	optional root complex and endpoint
Equalization Control	transceiver equalization controls
Control Interfaces	GUI and DCOM API
DC Supply Class External Adapter	15 V 10 A max 70 W class
Notes	
Numeric rows from Keysight U4305B Protocol Exerciser for PCI Express 3.0 data sheet and product literature.	

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.