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Data Sheet

August 14, 2026

ANRITSU

Anritsu ME7760A Wireless Communication Test System

The Anritsu ME7760A is a 25 to 43.5 Gbit/s bit-error-rate test system for 40 Gbit/s SONET/SDH modules and devices. OEM datasheet ME7760A-E-A-3 combines MP1775A 4-channel pulse pattern generator, MP1776A 4-channel error detector, MP1801A 43.5G MUX, MP1802A 43.5G DEMUX, and an external 68C/69B-family synthesized clock source under MX177601A SDH/SONET pattern editor control. OC-768/STM-256 and FEC/non-FEC 40G electrical/optical BER characterization of systems, modules, and MUX/DEMUX devices. 25 to 43.5 Gbit/s multiplexed BER testing Clock Source Family: Anritsu 68C or 69B synthesized signal generator required Mp1801a Dimensions Mass: 213 × 132.5 × 350 mm less than or equal to 8 kg Mp1775a Dimensions Mass: 426 × 221 × 450 mm less than or equal to 35 kg Literature: Anritsu ME7760A catalog ME7760A-E-A-3



MODEL

Anritsu ME7760A

CALIBRATION

Available on request

CONDITION

Used

STATUS

In stock

RFQ / SKU

ME7760A

LISTING

<https://aumictechlabs.com/products/me7760a-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Anritsu ME7760A is a versatile Bit Error Rate (BER) test solution designed for the evaluation of high-speed digital communication systems and components, particularly those operating at OC-768/STM-256 rates. This system is engineered to provide high-quality waveform output with low

jitter and minimal distortion, crucial for verifying and characterizing electrical and optical devices and modules that support Forward Error Correction (FEC), non-FEC, and Super FEC rates ranging from 25 Gbps to 43.5 Gbps. The ME7760A system is composed of multiple hardware elements and runs on PC-based software, offering flexibility for standalone use of individual instruments or combined configurations to meet specific testing requirements. Key Technical Specifications of the Anritsu ME7760A Bit Error Rate Testing Capabilities:

- * Operating Frequency Range: * 25 Gbps to 43.5 Gbps (covering standard FEC and non-FEC rates)
- * For the Pulse Pattern Generator (MP1775A) and Error Detector (MP1776A): 100 Mbps to 12.5 Gbps

System Configuration: Comprised of five hardware elements plus PC-based software.

Pulse Pattern Generator (MP1775A):

- * Generates four channels of SDH/SONET patterns or PRBS patterns.
- * Can generate PRBS patterns up to 43.5 Gbps, with selectable pattern lengths ($2^n - 1$, where $n = 7, 9, 11, 15, 20, 23, 31$).
- * Capable of generating 32 Mbits programmable patterns (user-defined).
- * Each channel can output signals up to 12.5 Gbps.
- * Features independent level adjustment for each of the 4 channels.
- * Supports 40 Gbps optical system testing when used with Anritsu 40G O/E and E/O Converters.

Error Detector (MP1776A):

- * Features four independent error detector channels.
- * Each channel can measure BER on signals up to 12.5 Gbps.
- * Can operate in independent mode or a 4-channel combined mode for optimal 43.5 Gbps data input evaluation.

Multiplexer/Demultiplexer: * MP1801A (MUX) and MP1802A (DEMUX) for the ME7760A system.

- * MP1801A can multiplex up to 4 data signal inputs (each up to 10.875 Gbps) to generate a 43.5 Gbps signal.
- * MP1802A can de-multiplex a 43.5 Gbps data input into 4 signals.
- * Supports 4:1 MUX and 1:4 DEMUX testing.

Pattern Generation:

- * Pure PRBS patterns.
- * Programmable patterns, including PRBS and inverted PRBS.
- * Testing of SONET/SDH frames up to OC-768c/STM-256c.
- * CID Pattern generation using MX177601A software.
- * 32 Mbits pattern memory for OC-768/STM-256.

Waveform Quality:

- * High-quality output waveforms with low jitter and low distortion.
- * High output amplitude: 2Vp-p.
- * Fast rise/fall times.

Forward Error Correction (FEC) Support: Capable of treating FEC signals on 40 Gbps.

System Requirements:

- * Computer: IBM-PC/AT compatible.
- CPU: Pentium 200 MHz or higher.
- Operating System: Windows 95/98/2000/NT4.0.
- Memory: 128 MB or more.
- Storage: 100 MB or more hard drive space required.
- Display: 800×600 resolution or higher, 256 colors or more.
- Interface: GPIB interface required (e.g., National Instruments PCMCIA-GPIB or AT-GPIB/TNT series).
- Clock Source: Requires an Anritsu 68C or 69B family signal generator (e.g., MG3690B Series) for clock signal generation.

Software:

- * MX177601A SDH/SONET Pattern Editor: * Used for editing pattern data.
- * Supports frame repetition (max 6 frames).
- * Alarm addition conforming to SDH/SONET standards (e.g., OOF/LOF, MS-AIS, MS-RDI, MS-REI).
- * BIP error addition and calculation (B1, B2, B3).
- * Scramble ON/OFF.
- * OH editor allows editing of all bytes except B1, B2, B3, H1, H2, H3.

Physical Characteristics:

- * Dimensions: 426 mm (W) x 266 mm (H) x 584 mm (D).
- Weight: Up to 50 kg (with 4 units of MU177601B).
- Operating Temperature: +15°C to +35°C.

System Components: The Anritsu ME7760A/B 43.5 Gbit/s BERT Systems are typically composed of the following elements, though the ME7760A is a lower-cost version:

- Signal Generator (e.g., Anritsu MG3690B Series)
- Pulse Pattern Generator (MP1775A)
- 4:1 Multiplexer (MP1801A for ME7760A system)
- 1:4 Demultiplexer (MP1802A for ME7760A system)
- Error Detector (MP1776A)
- PC

ME7760A Characteristics / Specifications

PARAMETER	VALUE
Instrument Type	43.5 Gbit/s BERT system
System Bit Rate Range	25 Gbit/s to 43.5 Gbit/s
Parallel Channel Rate	100 Mbit/s to 12.5 Gbit/s on MP1775A/MP1776A
Mux Model Me7760a	MP1801A 43.5G MUX
Demux Model Me7760a	MP1802A 43.5G DEMUX
Pulse Pattern Generator	MP1775A 4 channel
Error Detector	MP1776A 4 channel
Pattern Editor Software	MX177601A
Prbs Lengths	2^{n-1} for n=7,9,11,15,20,23,31
Mp1801a Operation Frequency	25 GHz to 43.5 GHz
Mp1801a Data Output Amplitude	2.0 Vp-p AC coupling fixed
Mp1801a Data Tr Tf	less than or equal to 18 ps (10-90 percent)
Mp1801a Pattern Jitter	less than or equal to 10 ps
Mp1801a Connector Data	V-connector
Mp1802a Data Input Amplitude	0.1 Vp-p to 1.0 Vp-p
Mp1802a Threshold Voltage	plus 0.25 V to -0.75 V variable
Mp1775a Operation Frequency	100 MHz to 12.5 GHz
Mp1775a Programmable Pattern	max 8 Mbits x 4 channels
Mp1775a Data Amplitude	0.5 Vp-p to 2.0 Vp-p
Mp1776a Error Ratio Range	0.0000×10^{-16} to 1.0000×10^0
Mp1776a Threshold Voltage	-3.000 V to plus 1.750 V (1 mV step)
Clock Source Family	Anritsu 68C or 69B synthesized signal generator required
Mp1801a Dimensions Mass	213 × 132.5 × 350 mm less than or equal to 8 kg
Mp1775a Dimensions Mass	426 × 221 × 450 mm less than or equal to 35 kg
Literature	Anritsu ME7760A catalog ME7760A-E-A-3

ME7760A Specifications

PARAMETER	VALUE
Anritsu ME7760A 43.5 Gbit/s BERT System	Overview
Applications	OC-768/STM-256 and FEC/non-FEC 40G electrical/optical BER characterization of systems, modules, and MUX/DEMUX devices.
Key Features	25 to 43.5 Gbit/s multiplexed BER testing
Technical Specifications	Instrument Type: 43.5 Gbit/s BERT system

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
Specifications	
PARAMETER	VALUE
Instrument Type	43.5 Gbit/s BERT system
System Bit Rate Range	25 Gbit/s to 43.5 Gbit/s
Parallel Channel Rate	100 Mbit/s to 12.5 Gbit/s on MP1775A/MP1776A
Mux Model Me7760a	MP1801A 43.5G MUX
Demux Model Me7760a	MP1802A 43.5G DEMUX
Pulse Pattern Generator	MP1775A 4 channel
Error Detector	MP1776A 4 channel
Pattern Editor Software	MX177601A
Prbs Lengths	2^n-1 for n=7,9,11,15,20,23,31
Mp1801a Operation Frequency	25 GHz to 43.5 GHz
Mp1801a Data Output Amplitude	2.0 Vp-p AC coupling fixed
Mp1801a Data Tr Tf	less than or equal to 18 ps (10-90 percent)
Mp1801a Pattern Jitter	less than or equal to 10 ps
Mp1801a Connector Data	V-connector
Mp1802a Data Input Amplitude	0.1 Vp-p to 1.0 Vp-p
Mp1802a Threshold Voltage	plus 0.25 V to -0.75 V variable
Mp1775a Operation Frequency	100 MHz to 12.5 GHz
Mp1775a Programmable Pattern	max 8 Mbits x 4 channels
Mp1775a Data Amplitude	0.5 Vp-p to 2.0 Vp-p
Mp1776a Error Ratio Range	0.0000x10^-16 to 1.0000x10^0
Mp1776a Threshold Voltage	-3.000 V to plus 1.750 V (1 mV step)
Clock Source Family	Anritsu 68C or 69B synthesized signal generator required
Mp1801a Dimensions Mass	213 x 132.5 x 350 mm less than or equal to 8 kg
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Notes

From Anritsu ME7760A 43.5Gbit/s BERT System datasheet (Catalog No. ME7760A-E-A-3). ME7760A is the lower-cost system using MP1801A/MP1802A; ME7760B uses MP1803A/MP1804A.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

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NAICS 423690 · 811210 · 541380
Generated August 14, 2026

Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.