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Data Sheet
August 14, 2026

ANRITSU

Anritsu MP1763C 12.5GHz Pulse Pattern Generator

Low jitter low distortion waveform output 1/8 parallel output standard with 1/4 options Optional 1/4 differential data for XAUI class interfaces Series Family: Anritsu MP1763C / MP1764 BERTS 1/8 parallel output standard with 1/4 options Optional 1/4 differential data for XAUI class interfaces Series Family: Anritsu MP1763C / MP1764 BERTS Bit Rate Coverage Class: 50 Mbit/s to 12.5 Gbit/s

MODEL Anritsu MP1763C	CALIBRATION Available on request
CONDITION Used	STATUS In stock
RFQ / SKU MP1763C	LISTING https://aumictechlabs.com/products/mp1763c-2/

NIST-traceable cal · SAM registered · 30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Anritsu MP1763C is a Pulse Pattern Generator designed for the research and development of high-speed logic, ICs, and digital systems. It is capable of generating pulse patterns up to 12.5 GHz and is well-suited for testing high-speed digital communication systems and devices, including those in telecommunications and SAN markets. When used in conjunction with the Anritsu MP1764C or MP1764D Error Detector, it forms a Bit Error Rate Test Set (BERTS) that supports evaluation from R&D through manufacturing and production at speeds ranging from 50 Mbit/s to 12.5 Gbit/s. The MP1763C is recognized for its high-quality waveform, comprehensive frequency coverage, and advanced pattern generation capabilities, making it a valuable tool for

rigorous testing and analysis. Technical Specifications Core Performance: Frequency Range: 0.05 GHz to 12.5 GHz Data Patterns: Generates four types of pulse patterns: alternate, programmable, zero substitution, and pseudorandom. Pseudorandom Patterns: Includes seven 2^N-1 (N=7, 9, 11, 15, 20, 23, 31) pseudorandom patterns. The mark ratio for pseudorandom patterns can be selected from among 0/8, 1/8, 1/4, 1/2, 3/4, 7/8, and 8/8. Programmable Pattern Length: Capable of generating programmable data patterns up to 8 M bits. This allows for the generation of six frames of STM-64/STS-192. Waveform Quality: Produces a high-quality eye diagram with fast rise/fall times (less than 30 ps), low distortion (less than 10%), and low jitter (less than 20 ps p-p crossover jitter). A high Q factor (greater than 40 dB) is achievable. Output Quality: Waveform distortion is ≤15% or ≤150 mV, whichever is greater. Clock Generation (Option 01): Internal Clock Frequency Range: 0.05 GHz to 12.5 GHz SSB Phase Noise: * ≤–85 dBc/Hz (0.05 to 4 GHz) at 10 kHz offset, 1 Hz bandwidth * ≤–80 dBc/Hz (4 to 8 GHz) at 10 kHz offset, 1 Hz bandwidth * ≤–75 dBc/Hz (8 to 10 GHz) at 10 kHz offset, 1 Hz bandwidth * ≤–70 dBc/Hz (10 to 12.5 GHz) at 10 kHz offset, 1 Hz bandwidth Clock Delay: Variable delay function for clock signals, adjustable by ±500 ps in 1 ps steps. This enables measurement of time-dependent characteristics or phase margins. Low FM/PM-Noise Clock Generator: Features a low FM/PM-noise clock generator. Output Characteristics: Data Output Channels: Two data output channels (DATA and DATA). Clock Output Channels: Three clock output channels (CLOCK1, CLOCK1, CLOCK2). Parallel Output: Standard 1/8 parallel output. Options for 1/4 parallel output (MP1763C-03) and 1/4 differential output (MP1763C-08) are available. The 1/4 differential output is noted as an industry-first for a 12.5G BERT system, specifically for SAN market device applications. Differential Inputs: Supports differential inputs, essential for applications like XAUI, SFI-4P2 4-Lane devices, and PCI Express. Complementary Outputs: Provides complementary outputs for both data and clock signals. Amplitude: Data output amplitude is adjustable from 0.25 Vp-p to 2.0 Vp-p. Offset: DC offset is selectable, adjustable within ±2 V. This allows for measurement of amplitude and offset margins. Pulsing Capability: The MP1763C can be externally gated using the GATING INPUT (0/-1 Volt Logic, 0V = Data On, -1V = Data Off) for burst signal generation. Interfaces and Control: GPIB Interface: Conforms to IEEE 488.2 standard for automatic or remote measurement via an external controller. Floppy Disk Drive: Built-in 3.5-inch floppy disk drive for storing preset data and enabling rapid measurements. Memory Cards: Utilizes memory cards for storing data and programs, with a caution regarding handling to prevent data loss. Compatibility and Applications: Applications: Ideal for research and development of high-speed logic, ICs, digital systems, high-speed digital communication systems, telecommunication systems (STM-0/STS-1 to STM-64/STS-192), 10 GbE, OUT-2, and 4.25G Fibre Channel systems. Also suitable for SAN market device applications and optical submarine transmission systems. Companio

MP1763C Characteristics / Specifications

PARAMETER	VALUE
Instrument Type	Pulse pattern generator
Series Family	Anritsu MP1763C / MP1764 BERTS
Operation Frequency	0.05 to 12.5 GHz
Bit Rate Coverage Class	50 Mbit/s to 12.5 Gbit/s
Programmable Pattern Length	8 Mbit
Alternate Pattern Length	4 Mbit
PRBS Patterns	2^7 minus 1 to 2^31 minus 1
Data Output Amplitude	0.25 to 2.0 Vp-p in 2 mV steps
Data Output Offset	minus 2 to plus 2 V in 1 mV steps
Clock Delay Range	minus 500 to plus 500 ps in 1 ps steps
Rise Fall Time Typical 10 to 90 Percent	30 ps
Jitter Typical	10 ps peak to peak
Internal Clock Option 01 Range	50 MHz to 12.5 GHz in 1 kHz steps
Internal Clock SSB Phase Noise 0.05 to 4 GHz	minus 85 dBc/Hz or better at 10 kHz offset
Internal Clock SSB Phase Noise 4 to 8 GHz	minus 80 dBc/Hz or better
Internal Clock SSB Phase Noise 8 to 10 GHz	minus 75 dBc/Hz or better
Internal Clock SSB Phase Noise 10 to 12.5 GHz	minus 70 dBc/Hz or better
Parallel Output	1/8 standard
Connector Class	APC 3.5 family interfacesQFactor Back to Back Typical at 10 Gbit/s PRBS 2^23 minus 1: 40 dB
Burst Generation	external gate supported
Polarity	DATA/DATA independently variable
Companion Error Detector	MP1764C / MP1764D

MP1763C Specifications

PARAMETER	VALUE
Key Features	Wideband PPG from 50 Mbit/s to 12.5 Gbit/s
Low jitter low distortion waveform output	1/8 parallel output standard with 1/4 options
Technical Specifications	Instrument Type: Pulse pattern generator
Notes	Numeric rows from Anritsu MP1763C/MP1764C/MP1764D PPG/ED datasheet.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

PARAMETER	VALUE
Instrument Type	Pulse pattern generator
Series Family	Anritsu MP1763C / MP1764 BERTS
Operation Frequency	0.05 to 12.5 GHz
Bit Rate Coverage Class	50 Mbit/s to 12.5 Gbit/s
Programmable Pattern Length	8 Mbit
Alternate Pattern Length	4 Mbit
PRBS Patterns	2^7 minus 1 to 2^31 minus 1
Data Output Amplitude	0.25 to 2.0 Vp-p in 2 mV steps
Data Output Offset	minus 2 to plus 2 V in 1 mV steps
Clock Delay Range	minus 500 to plus 500 ps in 1 ps steps

Rise Fall Time Typical 10 to 90 Percent: 30 ps
Jitter Typical: 10 ps peak to peak
Internal Clock Option 01 Range: 50 MHz to 12.5 GHz in 1 kHz steps
Internal Clock SSB Phase Noise 0.05 to 4 GHz: minus 85 dBc/Hz or better at 10 kHz offset
Internal Clock SSB Phase Noise 4 to 8 GHz: minus 80 dBc/Hz or better
Internal Clock SSB Phase Noise 8 to 10 GHz: minus 75 dBc/Hz or better
Internal Clock SSB Phase Noise 10 to 12.5 GHz: minus 70 dBc/Hz or better
Parallel Output: 1/8 standard
Option 03: 1/4 parallel output
Option 08: 1/4 differential data output 100 Mbit/s to 3.125 Gbit/s

Specifications

PARAMETER	VALUE
Connector Class	APC 3.5 family interfacesQFactor Back to Back Typical at 10 Gbit/s PRBS 2^23 minus 1: 40 dB
Burst Generation	external gate supported
Polarity	DATA/DATA independently variable
Companion Error Detector	MP1764C / MP1764D

Notes
Numeric rows from Anritsu MP1763C/MP1764C/MP1764D PPG/ED datasheet.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

Aumictech
788 S 500 E, Pleasant Grove, UT 84062
sales@aumictech.com · +1 (484) 841-9341
https://aumictechlabs.com

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