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**Data Sheet**
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ANRITSU

# Anritsu MP1764C 12.5GHz Error Detector

The Anritsu MP1764C is a 50 Mbit/s to 12.5 Gbit/s Error Detector used with the MP1763C Pulse Pattern Generator asaBERTS for evaluating transmission equipment, high-speed devices, and optical modules from R&D through manufacturing. It provides high input sensitivity, wide phase margin, auto-search for threshold/phase, eye-margin measurement, and optional differential input and clock recovery (MP1764D ships with those options installed). Supports STM-0/STS-1 through 10 GbE, STM-64/STS-192, OTU-2, and 4.25 Gbit/s Fibre Channel class rates. 12.5G BER testing of transmission equipment and optical modules; ultrahigh-speed logic IC R&D; ITU-T conformity evaluation; SAN/XAUI/SFI-4P2 differential device evaluation (with Opt. 02); Fibre Channel CDR evaluation (with Opt. 03); circulating-loop / burst measurements; eye-margin and Q-factor analysis (with software options). Instrument Type: Error Detector / BERTS receiver Family: MP1763C / MP1764C / MP1764D 50 Mbit/s to 12.5 Gbit/s BERTS Alias: MP1764C; Anritsu MP1764C; 12.5G Error Detector Threshold voltage variable range: −3.000 to +1.875 V (1 mV steps)

| MODEL | CALIBRATION |
|---|---|
| Anritsu MP1764C | Available on request |
| **CONDITION** | **STATUS** |
| Used | In stock |
| **RFQ / SKU** | **LISTING** |
| MP1764C | https://aumictechlabs.com/products/mp1764c-2/ |

NIST-traceable cal · SAM registered · 30-day returns

NAICS 423690 · 811210 · 541380

## This unit

Anritsu MP1764C,This high-speed error detector supports bit rates up to 12.5 GHz and is optimized for evaluating digital communications equipment. It features high sensitivity, low

intrinsic jitter, and fast synchronization, ensuring accurate bit error rate (BER) measurements in demanding test environments. The detector is ideal for verifying compliance of optical and electrical transmission systems, including SONET/SDH, Ethernet, and serial interfaces. Compatible with complementary pattern generators, it supports various test patterns and provides solid analysis through automatic error counting and pattern lock functions. The front panel offers intuitive controls, and the unit supports remote operation via GPIB for integration into automated test systems. Its low input threshold and high-frequency response ensure reliable detection even with degraded signals. The MP1764C is widely used in R&D, manufacturing, and compliance labs for confirming performance metrics of transmitters and receivers under real-world conditions. Compact and robust, it fits easily into standard test racks and offers excellent repeatability and measurement stability.

## Features & description

From manufacturer datasheet

### Features

• Operation frequency: 0.05 to 12.5 GHz • Input waveform: NRZ; input amplitude 0.25 to 2.0 Vp-p • Threshold voltage: −3.000 to +1.875 V in 1 mV steps • Input sensitivity: 50 mVp-p typical (10 Gbit/s, PRBS 2^23−1) • Phase margin: ≥70 ps typical (10 Gbit/s, PRBS 2^23−1, single-ended 1 Vp-p) • Auto-search for optimum input threshold and phase (one-touch) • PRBS patterns: 2^n−1 (n = 7, 9, 11, 15, 20, 23, 31) with mark ratios 1/2, 1/4, 1/8, 0/8 (logic inversion enables complementary ratios) • Programmable DATA pattern length: 2 to 8,388,608 bits • Alternate pattern A/B word length: 128 to 4,194,304 bits (128-bit steps) • Zero substitution: zero bit length 1 to (pattern length − 1); pattern length 2^n (n = 7, 9, 11, 15) • Sync modes: Normal, Frame, Quick; sync threshold preset or 10^−n (n = 2…8) • Error rate display range: 0.0000×10^−16 to 1.0000×10^0; error count 0 to 9.9999×10^16 • Eye margin measurement; error-performance DATA calculation; CH mask 1–32; block-window BER on 32-bit segments • CLOCK input delay: ±500 ps in 1 ps steps; polarity inversion; APC-3.5; terminate to GND or −2 V via 50 Ω • Optional MP1764C-02 Differential Data Input; MP1764C-03 Clock Recovery (62.5 Mbit/s–11.1 Gbit/s plus 4.25 Gbit/s Fibre Channel bands) • Optional MP1764C-01 Error Analysis (256-bit pattern around error bit) • Power ≤300 VA; operating temperature 0 to +50 °C • Dimensions/mass (base): 426 × 221.5 × 450 mm (W×H×D), ≤30 kg; with Opt. 02/03: 426 × 266 × 450 mm, ≤35 kg

## MP1764C Characteristics / Specifications

| PARAMETER | VALUE |
|---|---|
| **Model** | MP1764C |
| **Manufacturer** | Anritsu |
| **Instrument Type** | Error Detector / BERTS receiver |
| **Family** | MP1763C / MP1764C / MP1764D 50 Mbit/s to 12.5 Gbit/s BERTS |
| **Alias** | MP1764C; Anritsu MP1764C; 12.5G Error Detector DATA Input |
| **Operation frequency** | 0.05 to 12.5 GHz |
| **Input waveform** | rectangular (<0.5 GHz); rectangular or sine (≥0.5 GHz); duty 50% |
| **Input amplitude** | 0.25 to 2.0 Vp-p |
| **Threshold voltage variable range** | −3.000 to +1.875 V (1 mV steps) |
| **Phase margin** | ≥70 ps typical at 10 Gbit/s, PRBS 2^23−1, single-ended 1 Vp-p |
| **Input sensitivity** | 50 mVp-p typical at 10 Gbit/s, PRBS 2^23−1 |
| **Termination** | connected to GND or −2 V via 50 Ω |
| **Connector** | APC-3.5 Clock Recovery (Option MP1764C-03 / MP1764D) |
| **Input voltage** | 0.25 to 2.0 Vp-p |
| **Delay variable range** | ±500 ps (1 ps steps) |
| **Polarity** | CLOCK / CLOCK inversion possible |
| **CLOCK selection** | Internal / External |
| **Regenerated CLOCK output level** | 1.0 ±0.25 V (AC coupling) Minimum continuous 0 s tolerance (withstand) class per OEM table; 72 bit min. class for recovery lock conditions as published Receive Patterns |
| **PRBS** | 2^n−1 (n = 7, 9, 11, 15, 20, 23, 31) |
| **Mark ratio** | 1/2, 1/4, 1/8, 0/8 (1/2, 3/4, 7/8, 8/8 via logic inversion) |
| **DATA pattern length** | 2 to 8,388,608 bits |
| **Alternate A/B word length** | 128 to 4,194,304 bits (128-bit steps); loops via external signal |
| **Zero substitution** | 1 to (pattern length − 1) zeros; pattern length 2^n (n = 7, 9, 11, 15) Synchronization / Error Detection |
| **Synchronous mode** | Normal, Frame, Quick |

| PARAMETER | VALUE |
|---|---|
| **Synchronous threshold** | preset or 10^−n (n = 2, 3, 4, 5, 6, 7, 8) |
| **Error detection mode** | omission / insertion / total (rear DIP selectable) |
| **Quick sync example (OEM typical)** | sync gain ~850 ns at 10 Gbit/s, programmable pattern 2048 bits, sync threshold 10^−2 Measurement Items |
| **Error rate** | 0.0000×10^−16 to 1.0000×10^0 |
| **Number of errors** | 0 to 9.9999×10^16 |
| **Error interval (asynchronous)** | 0 to 9,999,999 (intervals 1 ms, 10 ms, 100 ms, 1 s) |
| **CLOCK frequency measurement** | 0.05 to 12.5 GHz; resolution 1 kHz; accuracy 10 ppm ±1 kHz |
| **Eye margin measurement** | provided |
| **Error performance DATA calculation** | provided |
| **Measurement CH mask** | 1 to 32 channels independently |
| **Block window** | error for any 32-bit segment block |
| **Error analysis Option** | stores 256 bits total before/after errored bit Auxiliary I/O |
| **Error output (direct)** | 1/128 OR error; 0/−1 V; SMA |
| **Error output (stretched)** | pulse width 350 ns typical; TTL; BNC |
| **Sync gain output** | 0/−1 V; SMA |
| **External mask / Resync inputs** | 0/−1 V; SMA |
| **Alternate A/B switching input** | ECL; SMA |
| **Sync signal output** | 1 (1/32 CLOCK, fixed or variable pattern position); 0/−1 V; SMA General |
| **Parameter memory** | 3.5-inch FD (2HD/2DD), MS-DOS Rev. 3.1 class; patterns/parameters |
| **Operating temperature** | 0 to +50 °C |
| **Power** | ≤300 VA |
| **EMC / LVD** | EN61326:1997/A2:2001 (Class A); EN61000-3-2:2000 (Class A); EN61010-1:2001 (Pollution Degree 2) Options |
| **MP1764D** | MP1764C with Opt. 02 and Opt. 03 installed |

| PARAMETER | VALUE |
| --- | --- |
| **Related software** | MX176400A Q/Eye Analysis; MX176401A SDH/SONET Pattern Editor; MX176403A GbE/10GbE Pattern Editor Notes Numeric specs from Anritsu MP1763C/MP1764C/MP1764D datasheet MP1763_64_E04 (2004). Confirm installed options (01/02/03) and whether unit is MP1764C vs MP1764D from labels. Pair with MP1763C PPG for full BERTS operation. |
| **Threshold voltage** | −3.000 to +1.875 V in 1 mV steps |
| **PRBS patterns** | 2^n−1 (n = 7, 9, 11, 15, 20, 23, 31) with mark ratios 1/2, 1/4, 1/8, 0/8 (logic inversion enables complementary ratios) |
| **Programmable DATA pattern length** | 2 to 8,388,608 bits |
| **Alternate pattern A/B word length** | 128 to 4,194,304 bits (128-bit steps) |
| **Sync modes** | Normal, Frame, Quick; sync threshold preset or 10^−n (n = 2…8) |
| **Error rate display range** | 0.0000×10^−16 to 1.0000×10^0; error count 0 to 9.9999×10^16 |
| **CLOCK input delay** | ±500 ps in 1 ps steps; polarity inversion; APC-3.5; terminate to GND or −2 V via 50 Ω |
| **Dimensions/mass (base)** | 426 × 221.5 × 450 mm (W×H×D), ≤30 kg; with Opt. 02/03: 426 × 266 × 450 mm, ≤35 kg |

## General Specifications & Supplementary Characteristics

| PARAMETER | VALUE |
|---|---|
| **Operating temperature** | 0 to +50 °C - Dimensions/mass (base): 426 × 221.5 × 450 mm (W×H×D), ≤30 kg; with Opt. 02/03: 426 × 266 × 450 mm, ≤35 kg |
| **Operating Temperature** | 0 to +50 °C - Dimensions/mass (base): 426 × 221.5 × 450 mm (W×H×D), ≤30 kg; with Opt. 02/03: 426 × 266 × 450 mm, ≤35 kg |
| **Model** | MP1764C |
| **Manufacturer** | Anritsu |
| **Instrument Type** | Error Detector / BERTS receiver |
| **Family** | MP1763C / MP1764C / MP1764D 50 Mbit/s to 12.5 Gbit/s BERTS |
| **Alias** | MP1764C; Anritsu MP1764C; 12.5G Error Detector DATA Input |
| **Operation frequency** | 0.05 to 12.5 GHz |
| **Input waveform** | rectangular (<0.5 GHz); rectangular or sine (≥0.5 GHz); duty 50% |
| **Input amplitude** | 0.25 to 2.0 Vp-p |
| **Threshold voltage variable range** | −3.000 to +1.875 V (1 mV steps) |
| **Phase margin** | ≥70 ps typical at 10 Gbit/s, PRBS 2^23−1, single-ended 1 Vp-p |
| **Input sensitivity** | 50 mVp-p typical at 10 Gbit/s, PRBS 2^23−1 |
| **Termination** | connected to GND or −2 V via 50 Ω |
| **Connector** | APC-3.5 Clock Recovery (Option MP1764C-03 / MP1764D) |
| **Input voltage** | 0.25 to 2.0 Vp-p |
| **Delay variable range** | ±500 ps (1 ps steps) |
| **Polarity** | CLOCK / CLOCK inversion possible |
| **CLOCK selection** | Internal / External |
| **Regenerated CLOCK output level** | 1.0 ±0.25 V (AC coupling) Minimum continuous 0 s tolerance (withstand) class per OEM table; 72 bit min. class for recovery lock conditions as published Receive Patterns |
| **PRBS** | 2^n−1 (n = 7, 9, 11, 15, 20, 23, 31) |
| **Mark ratio** | 1/2, 1/4, 1/8, 0/8 (1/2, 3/4, 7/8, 8/8 via logic inversion) |
| **DATA pattern length** | 2 to 8,388,608 bits |

| PARAMETER | VALUE |
|---|---|
| **Alternate A/B word length** | 128 to 4,194,304 bits (128-bit steps); loops via external signal |
| **Zero substitution** | 1 to (pattern length − 1) zeros; pattern length 2^n (n = 7, 9, 11, 15) Synchronization / Error Detection |
| **Synchronous mode** | Normal, Frame, Quick |
| **Synchronous threshold** | preset or 10^−n (n = 2, 3, 4, 5, 6, 7, 8) |
| **Error detection mode** | omission / insertion / total (rear DIP selectable) |
| **Quick sync example (OEM typical)** | sync gain ~850 ns at 10 Gbit/s, programmable pattern 2048 bits, sync threshold 10^−2 Measurement Items |
| **Error rate** | 0.0000×10^−16 to 1.0000×10^0 |
| **Number of errors** | 0 to 9.9999×10^16 |
| **Error interval (asynchronous)** | 0 to 9,999,999 (intervals 1 ms, 10 ms, 100 ms, 1 s) |
| **CLOCK frequency measurement** | 0.05 to 12.5 GHz; resolution 1 kHz; accuracy 10 ppm ±1 kHz |
| **Eye margin measurement** | provided |
| **Error performance DATA calculation** | provided |
| **Measurement CH mask** | 1 to 32 channels independently |
| **Block window** | error for any 32-bit segment block |
| **Error analysis Option** | stores 256 bits total before/after errored bit Auxiliary I/O |
| **Error output (direct)** | 1/128 OR error; 0/−1 V; SMA |
| **Error output (stretched)** | pulse width 350 ns typical; TTL; BNC |
| **Sync gain output** | 0/−1 V; SMA |
| **External mask / Resync inputs** | 0/−1 V; SMA |
| **Alternate A/B switching input** | ECL; SMA |
| **Sync signal output** | 1 (1/32 CLOCK, fixed or variable pattern position); 0/−1 V; SMA General |
| **Parameter memory** | 3.5-inch FD (2HD/2DD), MS-DOS Rev. 3.1 class; patterns/parameters |
| **Power** | ≤300 VA |
| **EMC / LVD** | EN61326:1997/A2:2001 (Class A); EN61000-3-2:2000 (Class A); EN61010-1:2001 (Pollution Degree 2) Options |
| **MP1764D** | MP1764C with Opt. 02 and Opt. 03 installed |

| PARAMETER | VALUE |
| --- | --- |
| **Related software** | MX176400A Q/Eye Analysis; MX176401A SDH/SONET Pattern Editor; MX176403A GbE/10GbE Pattern Editor Notes Numeric specs from Anritsu MP1763C/MP1764C/MP1764D datasheet MP1763_64_E04 (2004). Confirm installed options (01/02/03) and whether unit is MP1764C vs MP1764D from labels. Pair with MP1763C PPG for full BERTS operation. |

# Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

performance DATA calculation; CH mask 1–32; block-window BER on 32-bit segments
- CLOCK input delay: ±500 ps in 1 ps steps; polarity inversion; APC-3.5; terminate to GND or −2 V via 50 Ω
- Optional MP1764C-02 Differential Data Input; MP1764C-03 Clock Recovery (62.5 Mbit/s–11.1 Gbit/s plus 4.25 Gbit/s Fibre Channel bands)
- Optional MP1764C-01 Error Analysis (256-bit pattern around error bit)
- Power ≤300 VA; operating temperature 0 to +50 °C
- Dimensions/mass (base): 426 × 221.5 × 450 mm (W×H×D), ≤30 kg; with Opt. 02/03: 426 × 266 × 450 mm, ≤35 kg

Technical Specifications

### Technical Specifications

| PARAMETER | VALUE |
|---|---|
| **Model** | MP1764C |
| **Manufacturer** | Anritsu |
| **Instrument Type** | Error Detector / BERTS receiver |
| **Family** | MP1763C / MP1764C / MP1764D 50 Mbit/s to 12.5 Gbit/s BERTS |
| **Alias** | MP1764C; Anritsu MP1764C; 12.5G Error Detector |

DATA Input

### Specifications

| PARAMETER | VALUE |
|---|---|
| **Operation frequency** | 0.05 to 12.5 GHz |
| **Input waveform** | NRZ |
| **Input amplitude** | 0.25 to 2.0 Vp-p |
| **Threshold voltage variable range** | −3.000 to +1.875 V (1 mV steps) |
| **Phase margin** | ≥70 ps typical at 10 Gbit/s, PRBS 2^23−1, single-ended 1 Vp-p |
| **Input sensitivity** | 50 mVp-p typical at 10 Gbit/s, PRBS 2^23−1 |
| **Termination** | connected to GND or −2 V via 50 Ω |
| **Connector** | APC-3.5 |

Auto-search function: provided

CLOCK Input

### Specifications

| PARAMETER | VALUE |
|---|---|
| **Input waveform** | rectangular (<0.5 GHz); rectangular or sine (≥0.5 GHz); duty 50% |

| PARAMETER | VALUE |
|---|---|
| **Input voltage** | 0.25 to 2.0 Vp-p |
| **Delay variable range** | ±500 ps (1 ps steps) |
| **Polarity** | CLOCK / CLOCK inversion possible |
| **Termination** | GND or −2 V via 50 Ω |
| **Connector** | APC-3.5 |

Clock Recovery (Option MP1764C-03 / MP1764D)
Operation bit-rate bands: 62.5–100; 125–200; 250–400; 500–800; 1,000–1,600; 2,000–3,200 Mbit/s; 4,250 Mbit/s ±50 ppm; 9,900–11,100 Mbit/s
CLOCK selection: Internal / External
Regenerated CLOCK output level: 1.0 ±0.25 V (AC coupling)
Minimum continuous 0 s tolerance (withstand) class per OEM table; 72 bit min. class for recovery lock conditions as published

Receive Patterns
PRBS: 2^n−1 (n = 7, 9, 11, 15, 20, 23, 31)
Mark ratio: 1/2, 1/4, 1/8, 0/8 (1/2, 3/4, 7/8, 8/8 via logic inversion)
AND bit shift at mark-ratio setting: 1 or 3 bits (rear DIP selectable)

## Specifications

| PARAMETER | VALUE |
|---|---|
| **DATA pattern length** | 2 to 8,388,608 bits |
| **Alternate A/B word length** | 128 to 4,194,304 bits (128-bit steps); loops via external signal |
| **Zero substitution** | 1 to (pattern length − 1) zeros; pattern length 2^n (n = 7, 9, 11, 15) |

Synchronization / Error Detection

## Specifications

| PARAMETER | VALUE |
|---|---|
| **Synchronous mode** | Normal, Frame, Quick |
| **Synchronous threshold** | preset or 10^−n (n = 2, 3, 4, 5, 6, 7, 8) |
| **Error detection mode** | omission / insertion / total (rear DIP selectable) |
| **Quick sync example (OEM typical)** | sync gain ~850 ns at 10 Gbit/s, programmable pattern 2048 bits, sync threshold 10^−2 |

Measurement Items

## Specifications

| PARAMETER | VALUE |
|---|---|
| **Error rate** | 0.0000×10^−16 to 1.0000×10^0 |
| **Number of errors** | 0 to 9.9999×10^16 |
| **Error interval (asynchronous)** | 0 to 9,999,999 (intervals 1 ms, 10 ms, 100 ms, 1 s) |

Error-free interval (EFI): 0.0000% to 100.0000%

## Specifications

| PARAMETER | VALUE |
|---|---|
| **CLOCK frequency measurement** | 0.05 to 12.5 GHz; resolution 1 kHz; accuracy 10 ppm ±1 kHz |
| **Eye margin measurement** | provided |
| **Error performance DATA calculation** | provided |
| **Measurement CH mask** | 1 to 32 channels independently |
| **Block window** | error for any 32-bit segment block |
| **Error analysis Option 01** | stores 256 bits total before/after errored bit |

Auxiliary I/O
Error output (direct): 1/128 OR error; 0/−1 V; SMA
Error output (stretched): pulse width 350 ns typical; TTL; BNC
Alarm output (CLOCK loss, sync loss): TTL; BNC

## Specifications

| PARAMETER | VALUE |
|---|---|
| **Sync gain output** | 0/−1 V; SMA |
| **External mask / Resync inputs** | 0/−1 V; SMA |
| **Alternate A/B switching input** | ECL; SMA |
| **Sync signal output** | 1 (1/32 CLOCK, fixed or variable pattern position); 0/−1 V; SMA |

General
Parameter memory: 3.5-inch FD (2HD/2DD), MS-DOS Rev. 3.1 class; patterns/parameters
Operating temperature: 0 to +50 °C
Dimensions / mass (except Opt. 02, 03): 426 (W) × 221.5 (H) × 450 (D) mm; ≤30 kg
Dimensions / mass (Opt. 02, 03): 426 (W) × 266 (H) × 450 (D) mm; ≤35 kg
Power: ≤300 VA
EMC / LVD: EN61326:1997/A2:2001 (Class A); EN61000-3-2:2000 (Class A); EN61010-1:2001 (Pollution Degree 2)

Options
MP1764C-01: Error Analysis
MP1764C-02: Differential Data Input Function
MP1764C-03: Clock Recovery Function
MP1764D: MP1764C with Opt. 02 and Opt. 03 installed
Related software: MX176400A Q/Eye Analysis; MX176401A SDH/SONET Pattern Editor; MX176403A GbE/10GbE Pattern Editor

Notes
Numeric specs from Anritsu MP1763C/MP1764C/MP1764D datasheet MP1763_64_E04 (2004). Confirm installed options (01/02/03) and whether unit is MP1764C vs MP1764D from labels. Pair with MP1763C PPG for full BERTS operation.

## Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

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