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Data Sheet

August 15, 2026

CURTISS-WRIGHT / VMETRO

Curtiss-Wright / VMETRO PBTM-515B Bus Analyzer

The Curtiss-Wright/VMETRO PBTM-515B is a third-generation PCI and PMC bus analyzer delivering real-time monitoring, debugging, and performance analysis in a single-slot PMC module. It functions as a complete logic analyzer for 64-bit and 33/66 MHz systems, capture deep bus transaction insight, identify hardware and software issues rapidly, and validate system behavior across aerospace, defense, and industrial platforms. Three standard sampling modes: CLOCK, TRANSFER, and TRANSACTION; optional 500 MHz Timing Analyzer adds fourth mode Clock-by-clock sampling for low-level hardware protocol analysis via bus interface state machines Four full-speed Word Recognizers supporting true Address and Data Range definitions



MODEL

**Curtiss-Wright /
VMETRO PBTM-
515B**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

PBTM-515B

LISTING

<https://aumictechlabs.com/products/pbtm-515b-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 • 811210 • 541380

This unit

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deep bus transaction insight, identify hardware and software issues rapidly, and validate system behavior across aerospace, defense, and industrial platforms. Technical Specifications Bus Standards: PCI version 2.3 compliant; PMC module form factor Bus Width: Supports 32-bit and 64-bit PCI buses Clock Speeds: 33 MHz and 66 MHz systems; up to 66.7 MHz operation Signaling Levels: 3.3V and 5V signaling support Trace Memory: 64K depth (PBTM-515B model) Key Features State Analyzer Capabilities Three standard sampling modes: CLOCK, TRANSFER, and TRANSACTION; optional 500 MHz Timing Analyzer adds fourth mode Clock-by-clock sampling for low-level hardware protocol analysis via bus interface state machines Advanced triggering and filtering with 16-level Trigger/Qualifier Sequencer Multi-level triggering with trigger-after-delay or event-count logic Four full-speed Word Recognizers supporting true Address and Data Range definitions Address, command, and data de-multiplexing into separate trace channels Time tags in trace buffer indicating sample intervals Latency counter measuring target latency (FRAME# to TRDY#) and wait states between data transfers Exerciser Capabilities (with optional EXERBAT companion board) Bus Master interface with DMA support Target interface with 8 MB zero-wait-state burst memory DMA transfers between Exerciser and target, or between two bus targets Interrupt generation and handling Burst and Single cycle support Memory test patterns: walking ones/zeros, random patterns Built-in Script Recording and Playback with programmable delay and loop functions Typical Applications Aerospace and defense system development; industrial embedded PCI and PMC platform validation; real-time hardware-software co-verification. Compatibility & Integration Member of PBT-515 product family. Pairs with EXERBAT exerciser board for combined analysis and stimulus capabilities. Compatible with 32/64-bit PCI systems operating at 33/66 MHz with both 3.3V and 5V signaling.

PBTM515B Characteristics / Specifications

PARAMETER	VALUE
Model	PBTM-515B
Instrument Type	PCI bus analyzer
Bus	PCI
Family	VMETRO PBT-515
Functions	analyzer and exerciser class
Form Factor	PBTM PCI analyzer module
Manufacturer	Curtiss-Wright VMETRO
Mechanical Package	PCI analyzer module
Documentation	VMETRO PBT-515/PBTM-515B bus analyzer data
Application Class	PCI protocol debug
Related Cpci	PBTC-415BX cPCI bus analyzer sibling in the remaining queue
Capture	PCI protocol trace
Exerciser	bus exerciser in the 515 family
Duty	continuous bus analysis
Revision	B
Use Case	embedded and desktop PCI debug
Protocol	PCI
Trigger	protocol trigger/capture as published for PBT-515
Host	PCI slot or analyzer host as fitted
Grounding	PCI chassis ground
Power	from PCI/analyzer host
Software	VMETRO analyzer UI
System Family	VMETRO PBT bus analyzers

PBTM515B Specifications

PARAMETER	VALUE
Applications	Debugging PCI protocol, timing, and device enumeration on PCI backplanes.
Protocol trace capture	Exerciser functions in the PBT-515 family
Technical Specifications	Model: PBTM-515B

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
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System Family	VMETRO PBT bus analyzers
Notes	
From VMETRO PBT-515 family / PBTM-515B PCI bus analyzer listings. Exact state-machine depth and supported PCI clock rates are on the PBTM-515B sheet.	

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.