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Data Sheet

August 15, 2026

GE FANUC / ICS

GE Fanuc / ICS ICS-1555A-005 4-Channel, 160/180 MHz 16-bit ADC PMC Module with Virtex-5 SX95T User Programmable FPGA

GE Fanuc / ICS Data Acquisition Systems (DAQ). Voltage: 1.48 dBm (0.75 Vpp) or 5 dBm (1.125 Vpp), Bandwidth: 2 MHz to 300 MHz (-3 dB), Sample rate: 160 MHz or 180 MHz per channel.



MODEL

**GE Fanuc / ICS
ICS-1555A-005**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

ICS-1555A-005

LISTING

<https://aumictechlabs.com/products/ics-1555a-005-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The GE Fanuc / ICS ICS-1555A-005 is a 4-channel, 16-bit analog-to-digital converter (ADC) PMC module built around a user-programmable Xilinx Virtex-5 SX95T FPGA. It delivers simultaneous sampling at 160 MHz or 180 MHz per channel with AC-coupled 50 Ω inputs spanning 2 MHz to 300 MHz (-3 dB). The module integrates four Graychip GC4016 digital down-converters for flexible multi-band signal extraction and narrows signals to 10 MHz (-1 dB) per channel. Its PCI-X interface supports 64-bit/133 MHz master/target operation with burst-mode DMA, while 64 user I/Os connect directly to the FPGA via the Pn4 connector. Signal integrity is maintained with S/(N+D) ratios exceeding 73 dBFs at 160 MSPS and 70 dBFs at 180 MSPS, plus spurious-free dynamic range of 84 dBc at 70 MHz. Extended temperature variants are available. Technical Specifications Analog Inputs 4 channels, AC-coupled, 50 Ω input impedance Full-scale voltage:

1.48 dBm (0.75 Vpp) or 5 dBm (1.125 Vpp), software selectable Input bandwidth: 2 MHz to 300 MHz (-3 dB) Sample rate: 160 MHz or 180 MHz per channel; minimum 1 MHz Resolution: 16-bits Sampling Clock Internal: 100 MHz (Silicon Labs Si571) External: 32 MHz to 180 MHz, LVTTL/sinewave compatible External trigger: LVTTL/LVCMOS with 5V tolerance, edge-selectable External sync: LVTTL/sinewave, -3 dB min. to +6 dBm max. Digital Down-Converters 4× Graychip GC4016 devices Simultaneous down-conversion of up to 16 arbitrary signal bands Configuration: up to 16 narrowband, 8 split-I/Q, or 4 wideband channels Maximum output bandwidth: 10 MHz (-1 dB) per channel Arbitrary center frequency tuning within passband FPGA Xilinx Virtex-5 SX95T, user-programmable 36-Kbit block RAM/FIFOs, 25×18 DSP slices, SelectIO technology ChipSync interface blocks, system monitor, enhanced clock management with DCMs and PLLs Interfaces PCI-X: 64-bit/133 MHz, master/target, burst-mode DMA capable (PCI Local Bus Specification Revision 3.0, CMC/PMC P1386.1) User I/O: 64 lines via Pn4 connector (LVDS or LVTTL) Performance S/(N+D): >73 dBFs @ 70 MHz input, 160 MSPS; >70 dBFs @ 90 MHz input, 180 MSPS SFDR: 84 dBc @ 70 MHz input Key Features Multi-band signal extraction with four integrated digital down-converters Programmable FPGA for custom signal processing and control Flexible sampling clock (internal or external, 32–180 MHz) High dynamic range and low spurious content Typical Applications Communications signal analysis Radar data acquisition Test and measurement Compatibility & Integration PCI-X master/target interface with DMA capability integrates into standard CompactPCI and PMC carrier systems. Pn4 connector provides direct FPGA access for custom I/O protocols and signal routing.

ICS1555A005 Characteristics / Specifications

PARAMETER	VALUE
Model	ICS-1555A
Instrument Type	4 channel 16 bit ADC PMC digital receiver
Channel Count Maximum	4
ADC Resolution	16 bits
Sample Rate Option 1	160 MHz per channel
Example Dash Code 0	160 MHz 4 channel with DDCs
Analog Inputs	4 AC coupled
Input Impedance Class	50 ohm
DDC Devices Optional	4 x Graychip GC4016
Maximum Downconverted Bands	16
FPGA	Xilinx Virtex-5 SX95T
User IO	64 signals to FPGA
User IO Levels	LVDS or LVTTL
Form Factor	PMC
Host Interface Class	PCI-X 64 bit 133 MHz class
Clock Sync	external reference synchronization supported
Ruggedization Class	commercial benign
Primary Markets	communications radar test and measurement
Sibling Family	ICS-554 ICS-1554 legacy path
Dash 005 Meaning	160 MHz 4 channel with DDCs
Input Coupling	AC coupled
EOL Status Class	legacy end of life family

ICS1555A005 Specifications

PARAMETER	VALUE
Applications	Communications receivers, radar digitization, and test systems needing 16-bit high-rate PMC acquisition with onboard DDC and FPGA.
Key Features	Four 16 bit ADCs to 160 or 180 MHz
Optional four GC4016 DDCs for up to 16 bands	Virtex-5 SX95T user FPGA
Technical Specifications	Model: ICS-1555A
Notes	Numeric rows from Abaco ICS-1555 product page and ICS-1555A-005 configuration literature.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
Specifications	
PARAMETER	VALUE
Model	ICS-1555A
Instrument Type	4 channel 16 bit ADC PMC digital receiver
Channel Count Maximum	4
ADC Resolution	16 bits
Sample Rate Option 160	160 MHz per channel
Sample Rate Option 180	180 MHz per channel
Example Dash Code 005	160 MHz 4 channel with DDCs
Analog Inputs	4 AC coupled
Input Impedance Class	50 ohm
DDC Devices Optional	4 x Graychip GC4016
Maximum Downconverted Bands	16
FPGA	Xilinx Virtex-5 SX95T
User IO	64 signals to FPGA
User IO Levels	LVDS or LVTTL
Form Factor	PMC
Host Interface Class	PCI-X 64 bit 133 MHz class
Clock Sync	external reference synchronization supported
Ruggedization Class	commercial benign
Primary Markets	communications radar test and measurement
Sibling Family	ICS-554 ICS-1554 legacy path
Dash 005 Meaning	160 MHz 4 channel with DDCs
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EOL Status Class	legacy end of life family
Notes	
Numeric rows from Abaco ICS-1555 product page and ICS-1555A-005 configuration literature.	

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

788 S 500 E, Pleasant Grove, UT 84062
sales@aumictech.com · +1 (484) 841-9341
<https://aumictechlabs.com>

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.