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Data Sheet

August 12, 2026

HP / AGILENT

HP / Agilent 70001A W/ 70841B, 70842B Pattern Generator OPT H50

The HP/Agilent 70001A mainframe with 70841B Pattern Generator and 70842B Error Detector modules forms a modular digital communication test system operating from 50 MHz to 3 Gbit/s. This configuration delivers serial pattern generation, error detection, and bit-error-rate measurement across high-speed data channels. The 70001A 8-slot mainframe provides the infrastructure - power conditioning, cooling, MSIB module interconnect, and IEEE-488 control - enabling scalable test configurations within the HP Modular Measurement System architecture. Compatibility & Integration Modular System Interface Bus (MSIB) architecture enables integration with other HP 70000 Series MMS modules. Compatible with HP/Agilent 71603B Error Performance Analyzer. Supports both benchtop and standard EIA rack mounting. Aumictech offers NIST-traceable calibration and repair for the HP / Agilent 70001A / 70841B / 70842B

**MODEL****HP / Agilent
70001A / 70841B /
70842B****CALIBRATION****Available on
request****CONDITION****Used****STATUS****In stock****RFQ / SKU****70001A / 70841B /
70842B****LISTING**<https://aumictechlabs.com/products/70001a-70841b-70842b-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 • 811210 • 541380

This unit

The HP/Agilent 70001A mainframe with 70841B Pattern Generator and 70842B Error Detector modules forms a modular digital communication test system operating from 50 MHz to 3 Gbit/s. This configuration delivers serial pattern generation, error detection, and bit-error-rate measurement across high-speed data channels. The 70001A 8-slot mainframe provides the infrastructure - power conditioning, cooling, MSIB module interconnect, and IEEE-488 control - enabling scalable test configurations within the HP Modular Measurement System architecture.

Technical Specifications

Data rate range: 100 Mbit/s to 3 Gbit/s (70841B and 70842B)
Operating frequency: 50 MHz minimum (Option H50 enabled)
Pattern memory: 8192 bits internal per module; 4 Mbits disk storage per module
Mainframe architecture: 8-slot, supports 1/8-, 1/4-, 3/8-, and 1/2-width MMS plug-in modules
Power supply: Regulated 40 kHz AC to modules; 5 Vdc for MSIB; fan DC power; TTL line synchronization I/O ports (70841B): 8 total - six front panel, two rear panel I/O ports (70842B): 5 total - two front panel, three rear panel
Mainframe module slots: 418 MMS configuration
IEEE-488 (HP-IB) interface for external control and GPIB integration

Key Features

Pseudo-Random Binary Sequence generation: $2^{31}-1$, $2^{23}-1$, $2^{15}-1$, $2^{10}+1$, 2^7+1 with selectable polynomials
User-defined serial pattern capability with substitution of zeros to extend run lengths
Mark density control: 1/8, 1/4, 1/2, 3/4, 7/8 ratios of ones to total bits
Alternate pattern and word generation via rear-panel auxiliary input
Floppy disk drive integration for pattern storage and retrieval
Error detection and bit-error counting with reference pattern comparison
Option H50: Extends operating frequency floor to 50 MHz
EMC performance and field-proven structural design for laboratory and production environments

Typical Applications

High-speed serial data link characterization
BER measurement and eye diagram analysis
PRBS pattern-based compliance testing
Custom pattern generation for protocol-specific test sequences

Compatibility & Integration

Modular System Interface Bus (MSIB) architecture enables integration with other HP 70000 Series MMS modules. Compatible with HP/Agilent 71603B Error Performance Analyzer. Supports both benchtop and standard EIA rack mounting.

Features & description

From manufacturer datasheet

Features

- 70001A MMS mainframe hosts the modules
- 70841B: 4-slot pattern generator with PRBS, zero-substitution, mark-density, and user words
- 70842B: complementary 4-slot error detector with G.821-class analysis
- Option H50 lowers operating frequency to 50 Mb/s
- Front/rear I/O ports for clock and data paths
- Typically used with 70004A display and 70311A/70312A clock sources

Applications

- Multi-Gbit/s BER and error-performance analysis
- Serial PRBS and user-pattern generation for high-speed digital links
- Telecom / datacom component and system verification in MMS racks
- Extended low-rate testing with Option H50

70001A70841B70842B Characteristics / Specifications

PARAMETER	VALUE
Model	70001A / 70841B / 70842B
Manufacturer	HP / Agilent
Instrument Type	MMS Pattern Generator / Error Detector System
Alias	70001A; 70841B; 70842B; Opt H50; 71603B class
Mainframe	70001A MMS
Pattern generator	70841B
Error detector	70842B
Patterns	PRBS, zero substitution, variable mark density, user word
Error analysis basis	CCITT Rec. G.821 class measurements Notes Specs from HP 71600B / 70841B / 70842B literature for Opt H50 configurations. Confirm which modules and options are installed in the 70001A chassis; clock source and display modules may be separate line items.
70841B	4-slot pattern generator with PRBS, zero-substitution, mark-density, and user words
70842B	complementary 4-slot error detector with G.821-class analysis

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Performance Analyzer / 71604B Pattern Generator families. Option H50 extends low-end bit-rate operation down to 50 Mb/s (vs standard 100 Mb/s class).

Applications

- Multi-Gbit/s BER and error-performance analysis
- Serial PRBS and user-pattern generation for high-speed digital links
- Telecom / datacom component and system verification in MMS racks
- Extended low-rate testing with Option H50

Key Features

- 70001A MMS mainframe hosts the modules
- 70841B: 4-slot pattern generator with PRBS, zero-substitution, mark-density, and user words
- 70842B: complementary 4-slot error detector with G.821-class analysis
- Option H50 lowers operating frequency to 50 Mb/s
- Front/rear I/O ports for clock and data paths
- Typically used with 70004A display and 70311A/70312A clock sources

Technical Specifications

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PARAMETER	VALUE
Model	70001A / 70841B / 70842B
Manufacturer	HP / Agilent
Instrument Type	MMS Pattern Generator / Error Detector System
Alias	70001A; 70841B; 70842B; Opt H50; 71603B class

Specifications

PARAMETER	VALUE
Mainframe	70001A MMS
Pattern generator	70841B
Error detector	70842B

Option: H50 (extended low rate to 50 Mb/s)

70841B standard bit rate: 100 Mb/s to 3 Gb/s

70841B with H50 low end: 50 Mb/s

70842B standard bit rate: 100 Mb/s to 3 Gb/s

70842B with H50 low end: 50 Mb/s class

70841B module width: 4 MMS slots

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70841B data/clock jitter: less than 15 ps rms

70841B data transition 10% to 90%: less than 120 ps

70841B data transition 20% to 80%: less than 90 ps

70841B clock transition 10% to 90% at 3 GHz: less than 120 ps

Patterns: PRBS, zero substitution, variable mark density, user word

Error analysis basis: CCITT Rec. G.821 class measurements

Notes

Specs from HP 71600B / 70841B / 70842B literature for Opt H50 configurations. Confirm which modules and

options are installed in the 70001A chassis; clock source and display modules may be separate line items.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.