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Data Sheet

August 2, 2026

INTEL / WIND RIVER / EST

Intel / Wind River / EST VisionICE Scalable Emulator for PowerPC

Intel / Wind River / EST VisionICE Scalable Emulator for PowerPC The VisionICE provides a scalable in-circuit emulator designed for PowerPC development with MPC8xx-class BDM-style on-chip debug, supporting the full embedded lifecycle from chip evaluation through hardware/software integration, source-level debug, and production test. PowerPC chip and board bring-up; MPC8xx BDM-style on-chip debug sessions; hardware and software integration testing; source-level breakpoint debugging; production test and manufacturing programming; networked debug lab environments with optional Ethernet attachment. The VisionICE provides a scalable in-circuit emulator designed for PowerPC development with MPC8xx-class BDM-style on-chip debug, supporting the full embedded lifecycle from chip evaluation through hardware/software integration, source-level debug, and production test. PowerPC chip and board bring-up; MPC8xx BDM-style on-chip debug sessions; hardware and software integration testing; source-level breakpoint debugging; production test and manufacturing programming; networked debug lab environments with optional Ethernet attachment.



MODEL

**Intel / Wind River /
EST VisionICE**

CALIBRATION

**Available on
request**

CONDITION

Used

STATUS

In stock

RFQ / SKU

VisionICE

LISTING

<https://aumictechlabs.com/products/visionice-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 • 811210 • 541380

This unit

The Intel/Wind River/EST VisionICE Scalable Emulator for PowerPC is a modular emulation platform engineered for real-time debugging and performance analysis of embedded systems built on Motorola MPC8xx PowerPC processors. The system scales from entry-level Background Debug Mode (BDM) capabilities through visionCONTROL to advanced emulation and logic analysis via optional visionEVENT and visionNET modules. It delivers complete real-time debugging, hardware event isolation, precision trace buffering, and network-based remote debugging over Ethernet.

Technical Specifications

Processor Support: Motorola MPC8xx PowerPC family

Target Operating Voltage: 3.3V and 5V

Maximum Target Speed: 40 MHz

Hardware Breakpoints: 64 × 132-bit configuration for processor interruption or trace buffer triggering

Real-time Trace Buffer: 128 Kbytes × 96-bit, fully selectable

Time Stamp Resolution: 48-bit

Overlay Memory: Up to 4 Mbytes of RAM in visionICE Pod Assembly

Key Features

- Hardware event system with event isolation
- Real-time trace and time-stamp capability for performance tuning
- On-chip debugging services leveraging MPC8xx core BDM architecture
- visionCONTROL module provides software breakpoints, memory/register access, and code performance profiling
- visionEVENT module enables high-end emulation and real-time logic analysis
- visionNET module delivers full Ethernet support for shared and remote debugging across LAN infrastructure

Significantly reduced download times for large software images to target systems

Typical Applications

- Complex embedded systems development and optimization
- Real-time kernel integration and validation
- Multi-processor debug scenarios requiring network-based access
- Performance characterization and timing analysis of PowerPC-based designs

Compatibility & Integration

- Supports Motorola MPC8xx microprocessor family across PGA and FQFP package types
- Direct plug-in visionICE Pod Assembly configuration
- Compatible with leading source-level debuggers and real-time kernels
- Diagnostic functions and automatic chip select initialization included

Features & description

From manufacturer datasheet

Features

- Scalable in-circuit emulator for PowerPC (MPC8xx BDM-style on-chip debug) • VisionCONTROL base control unit • Optional VisionNET Ethernet remote debug interface • Optional VisionEVENT trace and breakpoint expansion • VisionEVENT: 64 × 132-bit breakpoints • VisionEVENT: 128K × 96-bit real-time trace buffer • VisionEVENT: 48-bit timestamp • Full lifecycle support: chip eval, HW/SW integration, source debug, production test

VISIONICE Characteristics / Specifications

PARAMETER	VALUE
Model	VisionICE (EST VisionICE scalable emulator)
Manufacturer	Embedded Support Tools (EST); associated with Intel / Wind River ecosystem
Instrument Type	Scalable In-Circuit Emulator for PowerPC
Target Architecture	PowerPC (MPC8xx BDM-style on-chip debug)
Base Unit	VisionCONTROL
VisionEVENT Breakpoints	64 × 132-bit
VisionEVENT Timestamp	48-bit
Lifecycle Coverage	Chip evaluation, HW/SW integration, source debug, production test
Related Family	VisionICE II (distinct product line—confirm generation on label)
Alias	VisionICE Standard Operating Conditions Connect target via appropriate BDM/debug probe for MPC8xx-class PowerPC device. Configure VisionCONTROL and optional VisionNET/VisionEVENT per target voltage and clock requirements. Verify probe firmware compatibility with target silicon revision before production test deployment.
VisionICE is the original EST scalable emulator family	not VisionICE II unless explicitly confirmed on inventory label or configuration sheet. Optional VisionEVENT module is required for advanced real-time trace and expanded breakpoint capability. Alias VisionICE.
VisionEVENT	64 × 132-bit breakpoints
Full lifecycle support	chip eval, HW/SW integration, source debug, production test

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

PARAMETER	VALUE
Model	VisionICE (EST VisionICE scalable emulator)
Manufacturer	Embedded Support Tools (EST); associated with Intel / Wind River ecosystem
Instrument Type	Scalable In-Circuit Emulator for PowerPC
Target Architecture	PowerPC (MPC8xx BDM-style on-chip debug)
Base Unit	VisionCONTROL

Optional Networking: VisionNET Ethernet interface

Optional Trace/Breakpoint: VisionEVENT module

VisionEVENT Breakpoints: 64 × 132-bit

VisionEVENT Real-Time Trace: 128K × 96-bit

Specifications

PARAMETER	VALUE
VisionEVENT Timestamp	48-bit
Lifecycle Coverage	Chip evaluation, HW/SW integration, source debug, production test
Related Family	VisionICE II (distinct product line-confirm generation on label)
Alias	VisionICE

Standard Operating Conditions

Connect target via appropriate BDM/debug probe for MPC8xx-class PowerPC device. Configure VisionCONTROL and optional VisionNET/VisionEVENT per target voltage and clock requirements. Verify probe firmware compatibility with target silicon revision before production test deployment.

Operational Notes

VisionICE is the original EST scalable emulator family-not VisionICE II unless explicitly confirmed on inventory label or configuration sheet. Optional VisionEVENT module is required for advanced real-time trace and expanded breakpoint capability. Alias VisionICE.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.