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Data Sheet

August 15, 2026

INTERFACE TECHNOLOGY

Interface Technology SR5010 Timing / Control Module

Interface Technology SR5010 Timing Control Module The Interface Technology SR5010 is a timing/control module. OEM SR5010 listings describe a system timing and control card used in Interface Technology digital test / word-generator systems to distribute clocks, triggers, and sequence control to companion modules such as DT9110 daughter cards. Master timing and control in Interface Technology digital test mainframes. Literature: Interface Technology SR5010 timing/control listings The Interface Technology SR5010 is a timing/control module. OEM SR5010 listings describe a system timing and control card used in Interface Technology digital test / word-generator systems to distribute clocks, triggers, and sequence control to companion modules such as DT9110 daughter cards. Master timing and control in Interface Technology digital test mainframes. Literature: Interface Technology SR5010 timing/control listings Family: Interface Technology SR5000 timing



MODEL

Interface Technology SR5010

CALIBRATION

Available on request

CONDITION

Used

STATUS

In stock

RFQ / SKU

SR5010

LISTING

<https://aumictechlabs.com/products/sr5010-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Interface Technology SR5010 is a timing and control module for the SR5000 Digital Test Subsystem, delivering precise timing signals and real-time test sequence control at data rates up

to 50 MHz. Built on a dual-processor architecture, the System Processor manages VXI Bus messaging and SCPI command execution, while the Control Processor operates as the real-time digital test engine, handling conditional branching, looping, and logic analysis trigger evaluation.

Technical Specifications
Data Rate: Up to 50 MHz
Processors: Dual-processor architecture (System Processor and Control Processor)
Test Program Storage: 32 different test programs
Vector Depth: 64K vectors
I/O Expandability: Up to 640 Inputs and 640 Outputs
Power Requirements: - +5.0 V @ 5.5 A (27.5 W) - -5.2 V @ 0.8 A (4.16 W) - +12 V @ 0.2 A (2.40 W) - -12 V @ 0.2 A (2.40 W) - -2.0 V @ 0.2 A (0.40 W) Total Maximum: 36.86 W
VXI Bus Interface: IT9010M chipset; compliant with VXI Bus Specification Versions 1.3 and 1.4
Data Transfer: A32/D32 Binary Transfer protocol
Key Features
RAM-Backed and Algorithmic Pattern Generation modes
Programmable edge placement for data formatting precision 16 Trigger Sequences with multilevel triggering capability
Response Qualifier Trigger Words supporting up to 8 combinations per sequence
Conditional pattern looping and branching for dynamic test control
Message-based command structure for streamlined test program development
Trigger actions select between UUT response data or compare error data recording
Typical Applications
Automatic test equipment (ATE) environments requiring synchronized device control, digital pattern generation with real-time branching logic, and advanced trigger-based data acquisition across large I/O matrices.
Compatibility & Integration
C-size slot module designed for SR5000 Digital Test Subsystem integration. Controls up to 20 SR5050 CMOS I/O modules, enabling configurations up to 640 I/O pins. VXI Bus Master capability passes test parameters and data to SR5000 I/O modules via message-based command protocol.

SR5010 Characteristics / Specifications

PARAMETER	VALUE
Model	SR5010
Instrument Type	Timing / control module
Manufacturer	Interface Technology
Literature	Interface Technology SR5010 timing/control listings
Family	Interface Technology SR5000 timing
Brand Lineage	Interface Technology
Form Factor	system timing module
System Role	master timing and control
Application Class	digital test / word generator
Clock Class	system clock distribution
Trigger Class	trigger I/O on SR5010
Sequence Class	sequence control
Related Daughter	DT9110
Documentation Type	OEM SR5010 listing
Vendor Path	Interface Technology
Year Class	SR5010
Bus Class	Interface Technology system bus
Connector Class	per SR5010 front/rear
Control Class	timing/control
Io Class	clock/trigger
Power Class	per SR5010 backplane pins
Operating Mode	system master timing
Module Class	SR5010

SR5010 Specifications

PARAMETER	VALUE
Interface Technology SR5010 Timing Control Module	Overview
Applications	Master timing and control in Interface Technology digital test mainframes.
Key Features	SR5010 timing / control module
Clock and trigger distribution	Companion to DT9110 daughter cards
Technical Specifications	Model: SR5010

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications	
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Control Class	timing/control
Io Class	clock/trigger
Power Class	per SR5010 backplane pins
Operating Mode	system master timing
Module Class	SR5010
Notes	
Identity from Interface Technology SR5010 timing/control listings. Clock rates, trigger levels, and pinout are on the SR5010 module specification and are not guessed here.	

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: sales@aumictech.com · +1 (484) 841-9341

Aumictech

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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.