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Data Sheet
August 13, 2026

INTERFACE TECHNOLOGY

Interface Technology SR5020A TTL I/O Module

Interface Technology SR5020A TTL I/O VXI Module The Interface Technology SR5020A is a 50 MHz digital interface module with 32 TTL inputs and 32 TTL outputs. NSN 6625-01-553-6119 identifies it asaplug-in electrical unit used on the Benchtop Reconfigurable Automatic Tester (BRAT). Memory types include stimulus, output, tristate, algorithmic, response record, expect, and mask with 65500 vectors of depth. It is the A-revision of the SR5020 C-size VXI TTL I/O family: dual-processor 68030 plus real-time control engine, seven memory banks at full 50 MHz, NRZ/RZ/RONE/RTC/RI formats, 16-level state machine, nine comparators, and per-channel 16-bit CCITT CRC. The Interface Technology SR5020A is a 50 MHz digital interface module with 32 TTL inputs and 32 TTL outputs. NSN 6625-01-553-6119 identifies it asaplug-in electrical unit used on the Benchtop Reconfigurable Automatic Tester (BRAT). Memory types include stimulus, output, tristate, algorithmic, response record, expect, and mask with 65500 vectors of depth. It is the A-revision of the SR5020 C-size VXI TTL I/O family: dual-processor 68030 plus real-time control engine, seven memory banks at full 50 MHz, NRZ/RZ/RONE/RTC/RI formats, 16-level state machine, nine comparators, and per-channel 16-bit CCITT CRC. BRAT and other VXI digital functional test

MODEL **Interface Technology SR5020A**	CALIBRATION **Available on request**
CONDITION **Used**	STATUS **In stock**
RFQ / SKU **SR5020A**	LISTING **https://aumictechlabs.com/products/sr5020a-2/**

NIST-traceable cal · SAM registered · 30-day returns

NAICS 423690 · 811210 · 541380

This unit

The SR5020A is a TTL I/O module for VXI-based digital test systems, delivering 32 input and 32 output channels per card at full 50 MHz data rates. Built around a dual-processor architecture with seven 64K-vector memory banks, it generates and verifies complex stimulus patterns with 100 ps edge placement resolution. Up to 20 modules operate under a single SR5010 Timing/Control Module, scaling systems to 640 I/O pins. The module supports multiple output formats NRZ, RZ, RONE, RTC, and tristate - and incorporates per-channel 16-bit CCITT CRC signature analysis. Each group of eight output pins shares independent timing generator pairs, while response timing accommodates window compare with glitch detection. Technical Specifications I/O Configuration: 32 input pins, 32 output pins per module Maximum System Capacity: 640 I/O pins (20 SR5020A modules + 1 SR5010 controller) Data Rate: 50 MHz Pattern Memory: Seven banks at 64K vectors deep Memory Types: Output, Algorithmic, Tristate, Expect, Mask, and Record patterns Edge Resolution: 100 ps Stimulus Timing Generators: 16 per module; grouped in sets of 2 pairs per 8 output pins Response Timing Generators: 2 per module (combinable for window compare) Signature Analysis: 16-bit CCITT CRC per input channel Output Formats: NRZ, RZ, RONE, RTC, RI (tristate) Power Consumption: 77.2 W at 50 MHz Key Features Pattern generation with algorithmic and RAM-backed modes Flexible stimulus and response timing with independent generator sets High-resolution edge placement for precise UUT synchronization Integrated signature analysis for response validation Modular expansion - stack up to 20 cards in one system Glitch detection within response timing window Electrical Requirements +5.0 V @ 10.0 A (50 W at 50 MHz) -5.2 V @ 4.0 A (20.8 W) +12.0 V @ 0.1 A (1.2 W) -12.0 V @ 0.1 A (1.2 W) -2.0 V @ 2.0 A (4.0 W) Compatibility & Integration Requires VXI mainframe and SR5010 Timing/Control Module supervision. Operates within standard VXI bus architecture for industrial and automotive digital functional test environments.

SR5020A Characteristics / Specifications

PARAMETER	VALUE
Model	SR5020A
Manufacturer	Interface Technology Inc (CAGE 5J927)
Instrument Type	VXI TTL digital I/O / pattern module
Family	SR5000 / SR5020 TTL I/O
Alias	SR 5020A; NSN 6625 01 553 6119
NSN Item Name	plug in unit electrical
End Item	Benchtop Reconfigurable Automatic Tester (BRAT)
Data Rate	50 MHz
Input Pins	32
Output Pins	32
Memory Depth	65500 vectors
Memory Types	stimulus; output; tristate; algorithmic; response record; expect; mask
Operating Temperature	0 C to +45 C
Storage Temperature	-40 C to +75 C
VXI Form Factor	C size, single slot (SR5020 family)
System Processor	68030 at 25 MHz (SR5020 family)
VXI Interface	message based to Slot 0 controller
Control Processor	real time digital test engine
Memory Banks Family	7 at 64K class / 65500 vectors
Stimulus Memories	output, algorithmic, tristate
Response Memories	expect, algorithmic, mask
Record Memory	UUT response or compare result
State Machine Levels	16 (family)
Digital Comparators	9 system wide (family)
CRC Register	16 bit CCITT per input channel (family)

PARAMETER	VALUE
Output Formats	NRZ, RZ, RONE, RTC, RI
Pattern Modes	RAM backed and algorithmic
Logic Family	TTL
Related SR5020 NSN	5998 01 458 4968
FSC	6625 Electrical and Electronic Properties Measuring and Testing Instruments
INC	66495

General Specifications & Supplementary Characteristics

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FSC	6625 Electrical and Electronic Properties Measuring and Testing Instruments
INC	66495 Notes Pin count, rate, vector depth, and temperature from NSN 6625-01-553-6119 characteristics. Dual-processor/memory-bank architecture is the published SR5020 family description and applies to theAmodule unless the faceplate firmware states otherwise. Timing-edge and voltage-level tables were not in the NSN extract; use the Interface Technology SR5020/SR5020A data sheet for those.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

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Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

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