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Data Sheet
August 2, 2026

STANFORD RESEARCH SYSTEMS

Stanford Research CG640 – CMOS (+5Vcc) up to 100MHz

Stanford Research CG640 – CMOS (+5Vcc) up to 100MHz The Stanford Research Systems CG640 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG640 converts the CG635 rear-panel clock output into +5 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 2.0 ns transition time, and an OEM maximum frequency Fmax of 105 MHz at specification (catalog titles may cite up to 100 MHz; output is set to logic 0 above Fmax). The Stanford Research Systems CG640 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG640 converts the CG635 rear-panel clock output into +5 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 2.0 ns transition time, and an OEM maximum frequency Fmax of 105 MHz at specification (catalog titles may cite up to 100 MHz; output is set to logic 0 above Fmax). Delivering +5 V CMOS clock signals to legacy and 5 V digital systems; remote clock distribution fromaCG635 master near the device under test; 5 V CMOS drive for microcontrollers, memory interfaces, and general digital test fixtures.

MODEL **Stanford Research Systems CG640**	CALIBRATION **Available on request**
CONDITION **Used**	STATUS **In stock**
RFQ / SKU **CG640**	LISTING **https://aumictechlabs.com/products/cg640-2/**

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NAICS 423690 · 811210 · 541380

This unit

The Stanford Research Systems CG640 is a CMOS clock generator delivering stable, precise clock signals up to 100 MHz from a +5Vcc power supply. Built for research laboratories, industrial automation, and system integration, the CG640 provides a dedicated clock source where timing accuracy and signal integrity are critical to system performance.Technical Specifications Output Frequency Range: Up to 100 MHz Output Type: CMOS Power Supply: +5VccKey Features clock signal generation with precise frequency control CMOS output architecture compatible with standard digital logic families Single +5Vcc supply operation simplifies power distribution and reduces system complexityTypical Applications Research laboratory instrumentation and test systems Industrial automation controllers requiring synchronized timing System integration in digital electronics requiring dedicated clock sources Applications demanding stable frequency generation up to 100 MHzCompatibility & Integration The +5Vcc power requirement ensures compatibility with legacy and modern laboratory and industrial equipment. Direct integration into systems using standard digital logic families is straightforward. The CMOS output format allows interface with TTL, CMOS, and ECL circuits depending on signal conditioning and impedance matching at the point of use.

Features & description

From manufacturer datasheet

Features

• CMOS (+5 Vcc) output adapter for CG635 • Complementary +CLK and −CLK on SMA connectors • 50 Ω source impedance; high-impedance load termination • Approximately 2.0 ns transition time (max) • Fmax 105 MHz at OEM specification • Output forced to logic 0 above Fmax • Connects via Category-6 cable to CG635 RJ-45 output • Remote placement away from the CG635 mainframe • Part of CG640–CG649 optional receiver family

CG640 Characteristics / Specifications

PARAMETER	VALUE
Stanford Research CG6	CMOS (+5Vcc) up to 100MHz Overview The Stanford Research Systems CG640 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG640 converts the CG635 rear-panel clock output into +5 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 2.0 ns transition time, and an OEM maximum frequency Fmax of 105 MHz at specification (catalog titles may cite up to 100 MHz; o
Model	CG640
Manufacturer	Stanford Research Systems
Instrument Type	Optional CMOS Output Adapter
Parent Instrument	CG635 Synthesized Clock Generator
Output Logic Family	CMOS (+5 Vcc)
Catalog Frequency Title	up to 100 MHz (marketing)
OEM Fmax at Specification	105 MHz
Behavior Above Fmax	output set to logic 0
Transition Time	approximately 2.0 ns (max)
Source Impedance	50 Ω
Load Impedance	High-Z (unterminated; terminating reduces amplitude by 2×)
Input	RJ-45; clock pair from CG635 via Category-6 cable (RS-485/LVDS path per CG635 rear panel)
Output	Complementary CMOS on SMA connectors
Power	supplied from CG635 rear-panel RJ-45 (±5 VDC for optional receivers) Standard Operating Conditions Use withaCG635 equipped for optional line receivers. Observe Category-6 cable length and quality versus frequency. CMOS outputs intended for high-impedance loads at end of coax when used per SRS guidance.
CG640 requiresaCG6	it cannot generate clocks independently. Unlike other CG64x receivers, CG640 does not continue with reduced amplitude above Fmax–the output goes to logic 0. Related CMOS adapters include CG641 (+3.3 Vcc, 250 MHz Fmax) and CG642 (+2.5 Vcc, 250 MHz Fmax). For PECL, ECL, RF, or LVDS levels, select other CG640–CG649 modules.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

PARAMETER	VALUE
Model	CG640
Manufacturer	Stanford Research Systems
Instrument Type	Optional CMOS Output Adapter
Parent Instrument	CG635 Synthesized Clock Generator
Output Logic Family	CMOS (+5 Vcc)
Catalog Frequency Title	up to 100 MHz (marketing)
OEM Fmax at Specification	105 MHz
Behavior Above Fmax	output set to logic 0
Transition Time	approximately 2.0 ns (max)
Source Impedance	50 Ω
Load Impedance	High-Z (unterminated; terminating reduces amplitude by 2×)
Input	RJ-45; clock pair from CG635 via Category-6 cable (RS-485/LVDS path per CG635 rear panel)
Output	Complementary CMOS on SMA connectors
Power	supplied from CG635 rear-panel RJ-45 (±5 VDC for optional receivers)

Standard Operating Conditions
Use withaCG635 equipped for optional line receivers. Observe Category-6 cable length and quality versus frequency. CMOS outputs intended for high-impedance loads at end of coax when used per SRS guidance.

Operational Notes
CG640 requiresaCG635–it cannot generate clocks independently. Unlike other CG64x receivers, CG640 does not continue with reduced amplitude above Fmax–the output goes to logic 0. Related CMOS adapters include CG641 (+3.3 Vcc, 250 MHz Fmax) and CG642 (+2.5 Vcc, 250 MHz Fmax). For PECL, ECL, RF, or LVDS levels, select other CG640–CG649 modules.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

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