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Data Sheet
August 2, 2026

STANFORD RESEARCH

Stanford Research CG641 – CMOS (+3.3Vcc) up to 500MHz

Stanford Research CG641 – CMOS (+3.3Vcc) up to 500MHz The Stanford Research Systems CG641 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG641 converts the CG635 rear-panel LVDS clock output into +3.3 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 800 ps transition time, and an OEM maximum frequency Fmax of 250 MHz at specification (catalog titles may cite up to 500 MHz; operation above 250 MHz continues with reduced amplitude). The Stanford Research Systems CG641 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG641 converts the CG635 rear-panel LVDS clock output into +3.3 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 800 ps transition time, and an OEM maximum frequency Fmax of 250 MHz at specification (catalog titles may cite up to 500 MHz; operation above 250 MHz continues with reduced amplitude). Delivering +3.3 V CMOS clock signals to modern digital ICs, FPGAs, and communications devices; remote clock distribution fromaCG635 master near the device under test; 3.3 V CMOS drive in high-speed digital test fixtures.

MODEL **Stanford Research CG641**	CALIBRATION **Available on request**
CONDITION **Used**	STATUS **In stock**
RFQ / SKU **CG641**	LISTING **https://aumictechlabs.com/products/cg641-2/**

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NAICS 423690 · 811210 · 541380

This unit

The Stanford Research CG641 is a CMOS clock generator delivering precision timing signals up to 500 MHz, powered by a single +3.3Vcc supply. The device outputs CMOS-level signals with 50 Ω output impedance designed for driving high-impedance loads across any length of 50 Ω coaxial cable. Transition times remain below 1 ns, enabling clean, fast clock edges for demanding synchronization requirements.Technical Specifications Maximum Frequency: 500 MHz Output Type: CMOS Power Supply: +3.3Vcc Output Impedance: 50 Ω Transition Times: Less than 1 ns Chassis Ground: AvailableKey Features Single +3.3 V supply simplifies integration into modern digital systems 50 Ω output impedance for controlled signal distribution via coaxial interconnects Sub-nanosecond transition times ensure minimal timing jitter Front-panel CMOS output connector for direct instrument accessTypical Applications The CG641 serves precision clock distribution in test benches, digital design validation, and laboratory measurement setups requiring stable, low-jitter reference signals at frequencies to 500 MHz.Compatibility & Integration Optional line receiver modules (CG640 to CG649 series) expand the CG641's functionality by providing complementary logic outputs on SMA connectors. These receivers accept independent ±5 VDC power delivered via rear-panel RJ-45 connector, allowing flexible multi-output configurations without additional external supplies.

Features & description

From manufacturer datasheet

Features

• CMOS (+3.3 Vcc) output adapter for CG635 • Complementary +CLK and −CLK on SMA connectors • 50 Ω source impedance; high-impedance load termination • Approximately 800 ps transition time (max) • Fmax 250 MHz at OEM specification • Connects via Category-6 cable to CG635 RJ-45 output • Remote placement away from the CG635 mainframe • Part of CG640–CG649 optional receiver family

CG641 Characteristics / Specifications

PARAMETER	VALUE
Stanford Research CG6	CMOS (+3.3Vcc) up to 500MHz Overview The Stanford Research Systems CG641 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG641 converts the CG635 rear-panel LVDS clock output into +3.3 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 800 ps transition time, and an OEM maximum frequency Fmax of 250 MHz at specification (catalog titles may cite up to 5
Model	CG641
Manufacturer	Stanford Research Systems
Instrument Type	Optional CMOS Output Adapter
Parent Instrument	CG635 Synthesized Clock Generator
Output Logic Family	CMOS (+3.3 Vcc)
Catalog Frequency Title	up to 500 MHz (marketing)
OEM Fmax at Specification	250 MHz
Behavior Above Fmax	continues operation with reduced amplitude
Transition Time	approximately 800 ps (max)
Source Impedance	50 Ω
Load Impedance	High-Z (unterminated; terminating reduces amplitude by 2×)
Input	RJ-45; LVDS clock pair from CG635 via Category-6 cable
Output	Complementary CMOS on SMA connectors
Power	supplied from CG635 rear-panel RJ-45 (±5 VDC for optional receivers) Standard Operating Conditions Use withaCG635 equipped for optional line receivers. Observe Category-6 cable length and quality versus frequency. CMOS outputs intended for high-impedance loads at end of coax when used per SRS guidance.
CG641 requiresaCG6	it cannot generate clocks independently. Catalog "500 MHz" titles reflect product family naming; verified OEM Fmax for in-spec operation is 250 MHz. Related CMOS adapters include CG640 (+5 Vcc, 105 MHz Fmax, logic 0 above Fmax) and CG642 (+2.5 Vcc, 250 MHz Fmax). For PECL, ECL, RF, or LVDS levels, select other CG640–CG649 modules.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

PARAMETER	VALUE
Model	CG641
Manufacturer	Stanford Research Systems
Instrument Type	Optional CMOS Output Adapter
Parent Instrument	CG635 Synthesized Clock Generator
Output Logic Family	CMOS (+3.3 Vcc)
Catalog Frequency Title	up to 500 MHz (marketing)
OEM Fmax at Specification	250 MHz
Behavior Above Fmax	continues operation with reduced amplitude
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Output	Complementary CMOS on SMA connectors
Power	supplied from CG635 rear-panel RJ-45 (±5 VDC for optional receivers)

Standard Operating Conditions
Use withaCG635 equipped for optional line receivers. Observe Category-6 cable length and quality versus frequency. CMOS outputs intended for high-impedance loads at end of coax when used per SRS guidance.

Operational Notes
CG641 requiresaCG635–it cannot generate clocks independently. Catalog "500 MHz" titles reflect product family naming; verified OEM Fmax for in-spec operation is 250 MHz. Related CMOS adapters include CG640 (+5 Vcc, 105 MHz Fmax, logic 0 above Fmax) and CG642 (+2.5 Vcc, 250 MHz Fmax). For PECL, ECL, RF, or LVDS levels, select other CG640–CG649 modules.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

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