Mon-Fri 8 AM - 6 PM ET    sales@aumictech.com | +1 (484) 841-9341

**Aumictech**

Test & measurement · bought, sold, repaired, calibrated

**Data Sheet**

August 2, 2026

STANFORD RESEARCH SYSTEMS

# Stanford Research CG642 – CMOS (+2.5Vcc) up to 500MHz

Stanford Research CG642 – CMOS (+2.5Vcc) up to 500MHz The Stanford Research Systems CG642 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG642 converts the CG635 rear-panel LVDS clock output into +2.5 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 800 ps transition time, and an OEM maximum frequency Fmax of 250 MHz at specification (catalog titles may cite up to 500 MHz; operation above 250 MHz continues with reduced amplitude). The Stanford Research Systems CG642 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG642 converts the CG635 rear-panel LVDS clock output into +2.5 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 800 ps transition time, and an OEM maximum frequency Fmax of 250 MHz at specification (catalog titles may cite up to 500 MHz; operation above 250 MHz continues with reduced amplitude). Delivering +2.5 V CMOS clock signals to low-voltage digital ICs and FPGA designs; remote clock distribution fromaCG635 master near the device under test; 2.5 V CMOS drive for communications and mixed-signal test fixtures.


| | |
|---|---|
| MODEL<br>Stanford Research Systems CG642 | CALIBRATION<br>Available on request |
| CONDITION<br>Used | STATUS<br>In stock |
| RFQ / SKU<br>CG642 | LISTING<br>https://aumictechlabs.com/products/cg642-2/ |

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

### This unit

The Stanford Research Systems CG642 is a CMOS clock generator engineered to produce stable, low-jitter clock signals at frequencies up to 500 MHz. Designed for demanding timing applications across advanced electronics, scientific instrumentation, and high-speed digital systems, this instrument delivers exceptional frequency stability from a single +2.5Vcc power supply.Technical Specifications Technology: CMOS Maximum Frequency: 500 MHz Power Supply Voltage: +2.5Vcc Output Interface: SMA connectors for high-frequency signal transmission Chassis Ground: Connected to outlet ground for electrical safetyKey Features Low-jitter clock signal generation frequency stability Single +2.5Vcc power supply operation SMA output connectors rated for frequencies to 500 MHzTypical Applications Advanced electronics timing and synchronization Scientific instrumentation requiring precision clocking High-speed digital system synchronization Laboratory environments demanding stable frequency referencesCompatibility & Integration SMA outputs require 50 Ω termination for optimal performance. The +2.5Vcc supply specification makes this generator compatible with modern low-voltage digital systems and mixed-signal applications where power efficiency is critical. Chassis ground connection ensures proper electrical isolation and safety compliance in bench and integrated system configurations.

## Features & description

From manufacturer datasheet

### Features

• CMOS (+2.5 Vcc) output adapter for CG635 • Complementary +CLK and −CLK on SMA connectors • 50 Ω source impedance; high-impedance load termination • Approximately 800 ps transition time (max) • Fmax 250 MHz at OEM specification • Connects via Category-6 cable to CG635 RJ-45 output • Remote placement away from the CG635 mainframe • Part of CG640–CG649 optional receiver family

## CG642 Characteristics / Specifications

| PARAMETER | VALUE |
| --- | --- |
| **Stanford Research CG6** | CMOS (+2.5Vcc) up to 500MHz Overview The Stanford Research Systems CG642 is an optional CMOS output receiver adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock source. The CG642 converts the CG635 rear-panel LVDS clock output into +2.5 V CMOS logic on complementary SMA outputs with 50 Ω source impedance and high-impedance load termination, approximately 800 ps transition time, and an OEM maximum frequency Fmax of 250 MHz at specification (catalog titles may cite up to 5 |
| **Model** | CG642 |
| **Manufacturer** | Stanford Research Systems |
| **Instrument Type** | Optional CMOS Output Adapter |
| **Parent Instrument** | CG635 Synthesized Clock Generator |
| **Output Logic Family** | CMOS (+2.5 Vcc) |
| **Catalog Frequency Title** | up to 500 MHz (marketing) |
| **OEM Fmax at Specification** | 250 MHz |
| **Behavior Above Fmax** | continues operation with reduced amplitude |
| **Transition Time** | approximately 800 ps (max) |
| **Source Impedance** | 50 Ω |
| **Load Impedance** | High-Z (unterminated; terminating reduces amplitude by 2×) |
| **Input** | RJ-45; LVDS clock pair from CG635 via Category-6 cable |
| **Output** | Complementary CMOS on SMA connectors |
| **Power** | supplied from CG635 rear-panel RJ-45 (±5 VDC for optional receivers) Standard Operating Conditions Use withaCG635 equipped for optional line receivers. Observe Category-6 cable length and quality versus frequency. CMOS outputs intended for high-impedance loads at end of coax when used per SRS guidance. |
| **CG642 requiresaCG6** | it cannot generate clocks independently. Catalog "500 MHz" titles reflect product family naming; verified OEM Fmax for in-spec operation is 250 MHz. Related CMOS adapters include CG640 (+5 Vcc, 105 MHz Fmax) and CG641 (+3.3 Vcc, 250 MHz Fmax). For PECL, ECL, RF, or LVDS levels, select other CG640–CG649 modules. |

# Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

## Specifications

| PARAMETER | VALUE |
|---|---|
| **Model** | CG642 |
| **Manufacturer** | Stanford Research Systems |
| **Instrument Type** | Optional CMOS Output Adapter |
| **Parent Instrument** | CG635 Synthesized Clock Generator |
| **Output Logic Family** | CMOS (+2.5 Vcc) |
| **Catalog Frequency Title** | up to 500 MHz (marketing) |
| **OEM Fmax at Specification** | 250 MHz |
| **Behavior Above Fmax** | continues operation with reduced amplitude |
| **Transition Time** | approximately 800 ps (max) |
| **Source Impedance** | 50 Ω |
| **Load Impedance** | High-Z (unterminated; terminating reduces amplitude by 2×) |
| **Input** | RJ-45; LVDS clock pair from CG635 via Category-6 cable |
| **Output** | Complementary CMOS on SMA connectors |
| **Power** | supplied from CG635 rear-panel RJ-45 (±5 VDC for optional receivers) |

Standard Operating Conditions
Use withaCG635 equipped for optional line receivers. Observe Category-6 cable length and quality versus frequency. CMOS outputs intended for high-impedance loads at end of coax when used per SRS guidance.

Operational Notes
CG642 requiresaCG635—it cannot generate clocks independently. Catalog "500 MHz" titles reflect product family naming; verified OEM Fmax for in-spec operation is 250 MHz. Related CMOS adapters include CG640 (+5 Vcc, 105 MHz Fmax) and CG641 (+3.3 Vcc, 250 MHz Fmax). For PECL, ECL, RF, or LVDS levels, select other CG640–CG649 modules.

## Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

**Aumictech**
788 S 500 E, Pleasant Grove, UT 84062
sales@aumictech.com · +1 (484) 841-9341
https://aumictechlabs.com

NIST-traceable calibration · SAM registered · 30-day returns
NAICS 423690 · 811210 · 541380
Generated August 2, 2026