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Data Sheet
August 2, 2026

STANFORD RESEARCH SYSTEMS

Stanford Research CG643 – PECL (+5Vcc) up to 2050MHz

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MODEL Stanford Research Systems CG643	CALIBRATION Available on request
CONDITION Used	STATUS In stock
RFQ / SKU CG643	LISTING https://aumictechlabs.com/products/cg643-2/

NIST-traceable cal · SAM registered · 30-day returns · NAICS 423690 · 811210 · 541380

This unit

The Stanford Research CG643 is a synthesized clock generator delivering PECL (+5Vcc) signals up to 2050 MHz for high-speed digital systems, communication networks, and test and measurement applications. This instrument combines exceptional frequency stability with flexible programmability, enabling precise clock edge positioning and dynamic timing control in demanding research and engineering environments.Technical Specifications Output Performance Output signal type: PECL (+5Vcc) Maximum output frequency: 2050 MHz Complementary square wave outputs Jitter (rms): Less than 1 ps across operational frequency range Transition time (rise/fall): 80 ps (20% to 80%) Frequency resolution: 16 digits Timing and Control Phase resolution: 1° for frequencies above 200 MHz Time modulation range: ±5 ns via rear-panel input Modulation sensitivity: 1 ns/V Modulation bandwidth: DC to over 10 kHz Configuration memory: 10 non-volatile storage slots Connectivity and References 10 MHz reference input (rear panel) 10 MHz reference output (rear panel) Accessory power: +5 V and −5 V (rear panel) Control interfaces: GPIB and RS-232 Power Supply Universal input AC power for worldwide operationKey Features High-precision PECL differential signaling for noise-immune clock distribution Sub-picosecond jitter performance for timing-critical applications Phase adjustment with 1° resolution above 200 MHz for exact clock edge positioning Dynamic time modulation capability enabling real-time timing adjustments Instant configuration recall from ten stored presets via memory function Accessory power outputs supporting remote clock receiver modules via Category-6 cableOptional Accessories Clock receiver modules for complementary high-speed transitions at standard logic levels on SMA connectors PRBS generator for random data pattern generation Multiple output types available including CMOS, ECL, LVDS, and RF through accessory modulesTypical Applications High-speed digital system synchronization, precision timing for communication networks, test and measurement instrument synchronization, and phase-coherent multi-channel signal generation in research laboratories.

Features & description

From manufacturer datasheet

Features

• PECL (+5 Vcc) output adapter for CG635 • Operates up to 2.05 GHz (2050 MHz) • 50 Ω source and load impedance • Approximately 100 ps transition times • Connects via Category-6 cable to CG635 RJ-45 output • Remote placement away from the CG635 mainframe • Part of CG640–CG649 optional receiver family

CG643 Characteristics / Specifications

PARAMETER	VALUE
Stanford Research CG6	PECL (+5Vcc) up to 2050MHz Overview The Stanford Research Systems CG643 is an optional PECL output adapter for the CG635 Synthesized Clock Generator–it is notastandalone clock generator. The CG643 converts the CG635 rear-panel LVDS clock output into PECL logic levels at +5 Vcc on 50 Ω outputs, operating to 2.05 GHz with approximately 100 ps transition times.
Model	CG643
Manufacturer	Stanford Research Systems
Instrument Type	Optional PECL Output Adapter
Parent Instrument	CG635 Synthesized Clock Generator
Output Logic Family	PECL (+5 Vcc)
Maximum Frequency	2.05 GHz (2050 MHz)
Transition Time	approximately 100 ps
Source Impedance	50 Ω
Load Impedance	50 Ω
Input	RJ-45; LVDS clock pair from CG635 via Category-6 cable
Output	PECL on SMA connector(s)
Power	supplied from CG635 rear-panel RJ-45 (±5 VDC for optional receivers) Standard Operating Conditions Use withaCG635 equipped for optional line receivers. Terminate PECL outputs with 50 Ω when required. Observe Category-6 cable length limits versus frequency (OEM guidance: shorter cables at higher frequencies).
CG643 requiresaCG6	it cannot generate clocks independently. Related PECL variants include CG644 (+3.3 Vcc) and CG645 (+2.5 Vcc). For RF or other logic families, select CG646 (RF +7 dBm), CG648 (ECL), or other CG640–CG649 modules per application.

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

PARAMETER	VALUE
Model	CG643
Manufacturer	Stanford Research Systems
Instrument Type	Optional PECL Output Adapter
Parent Instrument	CG635 Synthesized Clock Generator
Output Logic Family	PECL (+5 Vcc)
Maximum Frequency	2.05 GHz (2050 MHz)
Transition Time	approximately 100 ps
Source Impedance	50 Ω
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Input	RJ-45; LVDS clock pair from CG635 via Category-6 cable
Output	PECL on SMA connector(s)
Power	supplied from CG635 rear-panel RJ-45 (±5 VDC for optional receivers)

Standard Operating Conditions
Use withaCG635 equipped for optional line receivers. Terminate PECL outputs with 50 Ω when required. Observe Category-6 cable length limits versus frequency (OEM guidance: shorter cables at higher frequencies).

Operational Notes
CG643 requiresaCG635–it cannot generate clocks independently. Related PECL variants include CG644 (+3.3 Vcc) and CG645 (+2.5 Vcc). For RF or other logic families, select CG646 (RF +7 dBm), CG648 (ECL), or other CG640–CG649 modules per application.

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

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