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**Data Sheet**

August 2, 2026

## STANFORD RESEARCH SYSTEMS

## Stanford Research CG644 – PECL (+3.3Vcc) up to 2050MHz

Stanford Research CG644 – PECL (+3.3Vcc) up to 2050MHz The Stanford Research Systems CG644 is an optional PECL output adapter for the CG635 Synthesized Clock Generator—it is not a standalone clock generator. The CG644 converts the CG635 rear-panel LVDS clock output into PECL logic levels at +3.3 Vcc on 50  $\Omega$  outputs, operating to 2.05 GHz with approximately 100 ps transition times. It connects to the CG635 via Category-6 cable from the rear-panel RJ-45 interface, allowing remote placement of PECL clocks near the device under test. The Stanford Research Systems CG644 is an optional PECL output adapter for the CG635 Synthesized Clock Generator—it is not a standalone clock generator. The CG644 converts the CG635 rear-panel LVDS clock output into PECL logic levels at +3.3 Vcc on 50  $\Omega$  outputs, operating to 2.05 GHz with approximately 100 ps transition times. It connects to the CG635 via Category-6 cable from the rear-panel RJ-45 interface, allowing remote placement of PECL clocks near the device under test. Delivering clean PECL (+3.3 V) clock signals to high-speed digital and communications systems; remote clock distribution from a CG635 master; PECL drive for FPGAs, serializers, and communications ICs requiring 3.3 V PECL levels.



## MODEL

**Stanford Research  
Systems CG644**

## CALIBRATION

**Available on  
request**

## CONDITION

**Used**

## STATUS

**In stock**

## RFQ / SKU

**CG644**

## LISTING

<https://aumictechlabs.com/products/cg644-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 • 811210 • 541380

**This unit**

The Stanford Research Systems CG644 is a programmable PECL clock generator delivering stable, low-jitter signals up to 2050 MHz. Built on the proven CG635 Synthesized Clock Generator platform, it combines precise frequency control with fast transition times and exceptional timebase stability, making it ideal for high-speed digital system synchronization, test automation, and laboratory signal generation.

**Technical Specifications**

Frequency Range: DC to 2050 MHz  
Output Type: PECL (+3.3Vcc) Jitter (rms): <1 ps rms Transition Time (Rise/Fall): Typically 80 ps (20% to 80%)  
Frequency Resolution: 16 digits Output Impedance: 50  $\Omega$  (front-panel outputs); 100  $\Omega$  differential (rear-panel outputs)  
Load Impedance: 50  $\Omega$  (front-panel); 100  $\Omega$  differential (rear-panel)  
Timebase Stability: Better than 5 ppm (crystal standard); optional OCXO and Rubidium timebases available  
Power Supply: +3.3Vcc for PECL outputs; universal AC input worldwide; +5 V and -5 V accessory power on rear panel

**Key Features**

Complementary Q and -Q front-panel outputs for differential signaling  
Rear-panel RJ-45 connector supporting LVDS differential outputs to 2.05 GHz and RS-485 levels to 105 MHz CAT-6 cable compatible with 100  $\Omega$  terminations  
10 MHz reference input and output  
Phase and time modulation inputs  
GPIB and RS-232 remote control interfaces

**Typical Applications**

High-speed digital system clocking and synchronization  
Test and measurement equipment timing  
Data acquisition system synchronization  
RF and microwave instrumentation  
Laboratory clock generation

**Compatibility & Integration**

The CG644 integrates with standard 50  $\Omega$  and 100  $\Omega$  differential test infrastructure. Remote programming via GPIB or RS-232 enables seamless automation in ATE and laboratory environments. Optional precision timebases extend stability for demanding metrology applications.

## Features & description

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From manufacturer datasheet

### Features

- PECL (+3.3 Vcc) output adapter for CG635
- Operates up to 2.05 GHz (2050 MHz)
- 50  $\Omega$  source and load impedance
- Approximately 100 ps transition times
- Connects via Category-6 cable to CG635 RJ-45 output
- Remote placement away from the CG635 mainframe
- Part of CG640–CG649 optional receiver family

## CG644 Characteristics / Specifications

| PARAMETER             | VALUE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Stanford Research CG6 | PECL (+3.3Vcc) up to 2050MHz Overview The Stanford Research Systems CG644 is an optional PECL output adapter for the CG635 Synthesized Clock Generator—it is not a standalone clock generator. The CG644 converts the CG635 rear-panel LVDS clock output into PECL logic levels at +3.3 Vcc on 50 $\Omega$ outputs, operating to 2.05 GHz with approximately 100 ps transition times. It connects to the CG635 via Category-6 cable from the rear-panel RJ-45 interface, allowing remote placement of PECL clocks near the de |
| Model                 | CG644                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Manufacturer          | Stanford Research Systems                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Instrument Type       | Optional PECL Output Adapter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| Parent Instrument     | CG635 Synthesized Clock Generator                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| Output Logic Family   | PECL (+3.3 Vcc)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Maximum Frequency     | 2.05 GHz (2050 MHz)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Transition Time       | approximately 100 ps                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Source Impedance      | 50 $\Omega$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Load Impedance        | 50 $\Omega$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Input                 | RJ-45; LVDS clock pair from CG635 via Category-6 cable                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Output                | PECL on SMA connector(s)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Power                 | supplied from CG635 rear-panel RJ-45 (+/-5 VDC for optional receivers) Standard Operating Conditions Use with a CG635 equipped for optional line receivers. Terminate PECL outputs with 50 $\Omega$ when required. Observe Category-6 cable length limits versus frequency (OEM guidance: shorter cables at higher frequencies).                                                                                                                                                                                              |
| CG644 requires a CG6  | it cannot generate clocks independently. Related PECL variants include CG643 (+5 Vcc) and CG645 (+2.5 Vcc). For RF or other logic families, select CG646 (RF +7 dBm), CG648 (ECL), or other CG640–CG649 modules per application.                                                                                                                                                                                                                                                                                              |

# Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

| PARAMETER           | VALUE                                                                  |
|---------------------|------------------------------------------------------------------------|
| Model               | CG644                                                                  |
| Manufacturer        | Stanford Research Systems                                              |
| Instrument Type     | Optional PECL Output Adapter                                           |
| Parent Instrument   | CG635 Synthesized Clock Generator                                      |
| Output Logic Family | PECL (+3.3 Vcc)                                                        |
| Maximum Frequency   | 2.05 GHz (2050 MHz)                                                    |
| Transition Time     | approximately 100 ps                                                   |
| Source Impedance    | 50 $\Omega$                                                            |
| Load Impedance      | 50 $\Omega$                                                            |
| Input               | RJ-45; LVDS clock pair from CG635 via Category-6 cable                 |
| Output              | PECL on SMA connector(s)                                               |
| Power               | supplied from CG635 rear-panel RJ-45 (+/-5 VDC for optional receivers) |

Standard Operating Conditions

Use withaCG635 equipped for optional line receivers. Terminate PECL outputs with 50  $\Omega$  when required. Observe Category-6 cable length limits versus frequency (OEM guidance: shorter cables at higher frequencies).

Operational Notes

CG644 requiresaCG635—it cannot generate clocks independently. Related PECL variants include CG643 (+5 Vcc) and CG645 (+2.5 Vcc). For RF or other logic families, select CG646 (RF +7 dBm), CG648 (ECL), or other CG640–CG649 modules per application.

### Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: [sales@aumictech.com](mailto:sales@aumictech.com) · +1 (484) 841-9341

#### Aumictech

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NIST-traceable calibration · SAM registered ·  
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Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.