

**Aumictech**

Test &amp; measurement · bought, sold, repaired, calibrated

**Data Sheet**

August 2, 2026

STANFORD RESEARCH

## Stanford Research CG645 – PECL (+2.5Vcc) up to 2050MHz

Stanford Research CG645 – PECL (+2.5Vcc) up to 2050MHz The Stanford Research Systems CG645 is an optional PECL output adapter for the CG635 Synthesized Clock Generator—it is not a standalone clock generator. The CG645 converts the CG635 rear-panel LVDS clock output into PECL logic levels at +2.5 Vcc on 50  $\Omega$  outputs, operating to 2.05 GHz with approximately 100 ps transition times. Delivering clean PECL (+2.5 V) clock signals to low-voltage high-speed digital and communications systems; remote clock distribution from a CG635 master; PECL drive for FPGAs, serializers, and communications ICs requiring 2.5 V PECL levels. The Stanford Research Systems CG645 is an optional PECL output adapter for the CG635 Synthesized Clock Generator—it is not a standalone clock generator. The CG645 converts the CG635 rear-panel LVDS clock output into PECL logic levels at +2.5 Vcc on 50  $\Omega$  outputs, operating to 2.05 GHz with approximately 100 ps transition times. Delivering clean PECL (+2.5 V) clock signals to low-voltage high-speed digital and communications systems; remote clock distribution from a CG635 master; PECL drive for FPGAs, serializers, and communications ICs requiring 2.5 V PECL levels.



MODEL

**Stanford Research  
CG645**

CALIBRATION

**Available on  
request**

CONDITION

**Used**

STATUS

**In stock**

RFQ / SKU

**CG645**

LISTING

<https://aumictechlabs.com/products/cg645-2/>

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

**This unit**

The Stanford Research CG645 is a PECL clock generator delivering stable, precise timing signals up to 2050 MHz. Engineered for applications demanding stringent clock integrity - including high-speed digital systems, telecommunications infrastructure, and semiconductor testing - the CG645 provides the low-jitter outputs and clean spectral performance required in demanding laboratory and production environments.

**Technical Specifications**

Clock Generation Frequency range: Up to 2050 MHz  
Output signal type: PECL (+2.5Vcc)  
Output impedance: 50  $\Omega$   
Jitter (RMS): Typically < 1 ps rms  
Transition time: 80 ps (20% to 80%)  
Output Connectors: SMA connectors (standard on similar Stanford Research Systems instruments)

**Key Features**

- Sub-picosecond RMS jitter ensures timing fidelity in high-speed applications
- Fast edge transitions (80 ps) support clean clock distribution
- 50  $\Omega$  output impedance matches standard digital system interfaces
- PECL signaling provides low-noise differential outputs

**Typical Applications**

- High-speed digital system clocking
- Telecommunications and infrastructure timing
- Semiconductor device testing and characterization
- Advanced research laboratory instrumentation
- Systems requiring phase-coherent, low-jitter clock references

**Compatibility & Integration**

The CG645 operates as a standalone benchtop instrument. Rack-mount configuration options are available, enabling integration into automated test systems and facility-level timing distribution networks. PECL output levels and 50  $\Omega$  impedance ensure direct compatibility with digital logic families and high-speed data acquisition equipment.

## Features & description

---

From manufacturer datasheet

### Features

- PECL (+2.5 Vcc) output adapter for CG635
- Operates up to 2.05 GHz (2050 MHz)
- 50  $\Omega$  source and load impedance
- Approximately 100 ps transition times
- Connects via Category-6 cable to CG635 RJ-45 output
- Remote placement away from the CG635 mainframe
- Part of CG640–CG649 optional receiver family

## CG645 Characteristics / Specifications

| PARAMETER             | VALUE                                                                                                                                                                                                                                                                                                                                                                                 |
|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Stanford Research CG6 | PECL (+2.5Vcc) up to 2050MHz Overview The Stanford Research Systems CG645 is an optional PECL output adapter for the CG635 Synthesized Clock Generator—it is not a standalone clock generator. The CG645 converts the CG635 rear-panel LVDS clock output into PECL logic levels at +2.5 Vcc on 50 $\Omega$ outputs, operating to 2.05 GHz with approximately 100 ps transition times. |
| Model                 | CG645                                                                                                                                                                                                                                                                                                                                                                                 |
| Manufacturer          | Stanford Research Systems                                                                                                                                                                                                                                                                                                                                                             |
| Instrument Type       | Optional PECL Output Adapter                                                                                                                                                                                                                                                                                                                                                          |
| Parent Instrument     | CG635 Synthesized Clock Generator                                                                                                                                                                                                                                                                                                                                                     |
| Output Logic Family   | PECL (+2.5 Vcc)                                                                                                                                                                                                                                                                                                                                                                       |
| Maximum Frequency     | 2.05 GHz (2050 MHz)                                                                                                                                                                                                                                                                                                                                                                   |
| Transition Time       | approximately 100 ps                                                                                                                                                                                                                                                                                                                                                                  |
| Source Impedance      | 50 $\Omega$                                                                                                                                                                                                                                                                                                                                                                           |
| Load Impedance        | 50 $\Omega$                                                                                                                                                                                                                                                                                                                                                                           |
| Input                 | RJ-45; LVDS clock pair from CG635 via Category-6 cable                                                                                                                                                                                                                                                                                                                                |
| Output                | PECL on SMA connector(s)                                                                                                                                                                                                                                                                                                                                                              |
| Power                 | supplied from CG635 rear-panel RJ-45 ( $\pm 5$ VDC for optional receivers) Standard Operating Conditions Use with a CG635 equipped for optional line receivers. Terminate PECL outputs with 50 $\Omega$ when required. Observe Category-6 cable length limits versus frequency (OEM guidance: shorter cables at higher frequencies).                                                  |
| CG645 requires a CG6  | it cannot generate clocks independently. Related PECL variants include CG643 (+5 Vcc) and CG644 (+3.3 Vcc). For RF or other logic families, select CG646 (RF +7 dBm), CG648 (ECL), or other CG640–CG649 modules per application.                                                                                                                                                      |

# Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

| PARAMETER           | VALUE                                                                      |
|---------------------|----------------------------------------------------------------------------|
| Model               | CG645                                                                      |
| Manufacturer        | Stanford Research Systems                                                  |
| Instrument Type     | Optional PECL Output Adapter                                               |
| Parent Instrument   | CG635 Synthesized Clock Generator                                          |
| Output Logic Family | PECL (+2.5 Vcc)                                                            |
| Maximum Frequency   | 2.05 GHz (2050 MHz)                                                        |
| Transition Time     | approximately 100 ps                                                       |
| Source Impedance    | 50 $\Omega$                                                                |
| Load Impedance      | 50 $\Omega$                                                                |
| Input               | RJ-45; LVDS clock pair from CG635 via Category-6 cable                     |
| Output              | PECL on SMA connector(s)                                                   |
| Power               | supplied from CG635 rear-panel RJ-45 ( $\pm 5$ VDC for optional receivers) |

Standard Operating Conditions

Use withaCG635 equipped for optional line receivers. Terminate PECL outputs with 50  $\Omega$  when required. Observe Category-6 cable length limits versus frequency (OEM guidance: shorter cables at higher frequencies).

Operational Notes

CG645 requiresaCG635-it cannot generate clocks independently. Related PECL variants include CG643 (+5 Vcc) and CG644 (+3.3 Vcc). For RF or other logic families, select CG646 (RF +7 dBm), CG648 (ECL), or other CG640-CG649 modules per application.

### Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: [sales@aumictech.com](mailto:sales@aumictech.com) · +1 (484) 841-9341

#### Aumictech

788 S 500 E, Pleasant Grove, UT 84062  
[sales@aumictech.com](mailto:sales@aumictech.com) · +1 (484) 841-9341  
<https://aumictechlabs.com>

NIST-traceable calibration · SAM registered ·  
30-day returns  
NAICS 423690 · 811210 · 541380  
Generated August 2, 2026

Technical content from manufacturer specifications. Unit photo/stock from Aumictech listing when available. Specifications subject to OEM documentation and unit condition.