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Data Sheet
August 12, 2026

TEKTRONIX

# Tektronix BSA286CL BERTScope 28.6 Gb/s Bit Error Rate Analyzer

1×10 -12 directly. Either way, the BERTScope's one-button measurements are compliant to the MJSQ jitter methodology, and because the underlying delay control is the best available on any BERT you can be sure that the measurements are accurate. Use the built-in calculations for Total Jitter (TJ), Random Jitter (RJ), and Deterministic Jitter (DJ), or easily export the data and use your own favorite jitter model. The BSA286CL's low intrinsic RJ supports serving of 802.3ba's simultaneous VECP (Vertical Eye Closure Penalty) and J2/J9 calibration with valuable margin required to fully characterize 100G Ethernet silicon. Mask compliance contour testing Many standards such as XFP/XFI and OIF CEI now specify mask tests intended to assureaspecified 1×10 -12 eye opening. Compliance Contour view makes this easy by takingamask, and overlaying it on your measured BER contours - so you can immediately see whether you have passed the mask at whatever BER level you decide. Quick selection guide ModelMaximum bit rateStressed eye - SJ, RJ, BUJ, SI BSA286CL28.6 Gb/sOpt. STR BSA175C17.5 Gb/sOpt. STR BSA125C12.5 Gb/sOpt. STR Flexible clocking The generator clock path features in the BERTScope provides the test flexibility needed for emerging real-world devices. Whether computer cards or disk drives, it is often necessary to be able to provideasub-rate system clock, such as 100 MHz for PCI Express

No photo

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|---|---|
| MODEL<br>Tektronix BSA286CL | CALIBRATION<br>N/A — off-catalog OEM datasheet |
| CONDITION<br>See OEM documentation | STATUS<br>Not listed on Aumictech inventory |
| RFQ / SKU<br>BSA286CL | LISTING<br>Off-catalog — OEM dat asheet only |

NIST-traceable cal

SAM registered

30-day returns

NAICS 423690 · 811210 · 541380

## Features & description

From manufacturer datasheet

### Built-in jitter tolerance function

Datasheet 6 www.tek.com BERTScope pattern generators The BERTScope pattern generators provideafull range of PRBS patterns, common standards-based patterns, and user-defined patterns. Option STR provides full integrated, calibrated stress generation which is an easy-to-use alternative toarack full of manually calibrated instruments needed to provideastressed pattern. Uses include receiver testing of devices with internal BER measurement ability such as DisplayPort, or adding stress capability to legacy BERT instruments. Stressed eye option Pattern capture There are several methods for dealing with unknown incoming data. In addition to Live Data Analysis discussed above, a useful standard feature on all BERTScope analyzers is pattern capture. This allows the user to specify the length ofarepeating pattern and then allow the analyzer to grab the specified incoming data using the detector's 128 Mb RAM memory. This can then be used as the new detector reference pattern, or edited and saved for later use. Pattern capture Using the Power of Error Analysis – In the following example eye diagram views were linked with BER to identify and solveadesign issue inamemory chip controller. The eye diagram (top left) showsafeature in the crossing region that is unexpected and appearing less frequently than the main eye. Moving the BER decision point to explore the infrequent events is revealing. Error Analysis shows that the features are related in some way to the number 24. Further investigation traced the anomaly to clock breakthrough within the IC; the system clock was at 1/24th of the output data rate. Redesigning the chip with greater clock path isolation gave the clean waveform of the top right eye diagram.

## BSA286CL Characteristics / Specifications

| PARAMETER | VALUE |
|---|---|
| **Pattern capture Using the Power of Error Analysis** | In the following example eye diagram views were linked with BER to identify and solveadesign issue inamemory chip controller. The eye diagram (top left) showsafeature in the crossing region that is unexpected and appearing less frequently than the main eye. Moving the BER decision point to explore the infrequent events is revealing. Error Analysis shows that the features are related in some way to the number 24. Further investigation traced the anomaly to clock breakthrough within the IC; the sy |
| **Jitter map Features include** | DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data Dependent Jitter (DDJ), Inter-Symbol Interference (ISI), Duty Cycle Distortion (DCD), and Sub-Rate Jitter (SRJ) including F/2 (or F2) Jitter BER-based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10 –12 BER and beyond Separation of correlated and non-correlated jitter components eliminates mistaking long pattern DDJ for RJ |
| **Jitter impairments Bounded uncorrelated jitter** | Supports data rates from 1.5 to 12.5 Gb/s (BSA125C), 17.5 Gb/s (BSA175C), and 28.6 Gb/s (BSA286CL) with limited performance to 622 Mb/s (BSA286CL excluded) Internal PRBS Generator Variable up to 0.5 UI 100 Mb/s to 2.0 Gb/s Band-limited by selected filters BUJ rateFilter 100 to 499 25 MHz 500 to 999 50 MHz |
| **Eye diagrams** | 280×350 pixel waveform display Deep acquisition Automatic Measurements include: Rise time Fall time Unit interval (data, and also clock) Eye amplitude Noise level of 1 or 0 Eye width Eye height Eye jitter (p-p and RMS) 0 level, 1 level Extinction ratio Vertical eye closure penalty (VECP) Dark calibration Signal-to-Noise ratioVp-p , V |
| **Physical layer test option The following physical layer test options are available** | BER contour testing Executed with same acquisition circuitry as eye diagram measurements for maximum correlation As-needed delay calibration for accurate points Automatic scaling, one-button measurement Extrapolates contours from measured data, increasing measurement depth with run time and repeatedly updating curve fits Easy export of fitted data in CSV format |
| **Contours available from** | 6 to 10 –16 in decade steps Bit Error Rate Tester -- BERTScope ® BSA Series www.tek.com 11 Basic jitter measurements Testing to T11.2 MJSQ BERTScan methodology (also called ‘Bathtub Jitter’) Deep measurements for quick and accurate extrapolation of Total Jitter at user-specified level, or direct measurement Separation of Random and Deterministic components, as defined in MJSQ As-needed delay calibration for accurate points Export of points in CSV format Easy one-button measurement User-specified |

| PARAMETER | VALUE |
|---|---|
| **Many views come standard with the BERTScope Family** | Error statistics: A tabular display of bit and burst error counts and rates Error Statistics view showing link performance in terms of bit and burst occurrences. |
| **Strip chart** | A strip chart graph of bit and burst error rates Strip Chart view showing bit and burst error performance over time. This can useful while temperature cycling as part of troubleshooting. |
| **Burst length** | A histogram of the number of occurrences of errors of different lengths Error free interval: A histogram of the number of occurrences of different error-free intervals Correlation: A histogram showing how error locations correlate to userset block sizes or external marker signal inputs Pattern sensitivity: A histogram of the number of errors at each position of the bit sequence used as the test pattern |
| **Block errors** | A histogram showing the number of occurrences of data intervals (ofauser-set block size) with varying numbers of errors in them The Pattern Sensitivity view isapowerful way of examining whether error events are pattern related. It shows which pattern sequences are the most problematic, and operates on PRBS and user-defined patterns. |
| **Standard library of templates** | 10GBASE LX4 802.3ae 3.125 Gb/s 10 GbE 802.3ae 10.3125 Gb/s 40 GbE 802.3ba LR4 10.3125 Gb/s 100 GbE 802.3ba LR4/ER4 25.78125 Gb/s CEI 11G Datacom Rx Ingress (D) 11 Gb/s CGE Telecom Rx Egress (Re) 11 Gb/s 5 CEI 11G Telecom Rx Ingress (Ri) 11 Gb/s 5 CEI 11G Total Wander 11.1 Gb/s |
| **Some of the areas of adjustment include** | BER confidence level Test duration per point BER threshold Test device relaxation time Imposition of percentage margin onto template Test precision Control over A/B Pattern switch behavior Also included is the ability to test beyond the template to device failure at each chosen point, and the ability to export data either as screen images or |
| **The option includes the following features** | DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data Dependent Jitter (DDJ), Inter-Symbol Interference (ISI), Duty Cycle Distortion (DCD), and Sub-Rate Jitter (SRJ) 7 including F/2 (or F2) jitter BER based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10 –12 BER and beyond Separation of correlated and uncorrelated jitter components eliminates mistaking long pattern DDJ for RJ |
| **Maximum nondestructible input** | 3 V peak , +4 V peak , applied to any connector Detector clock data delay RangeGreater than 1 bit period in all cases Up to 1.1 GHz30 ns Above 1.1 GHz3 ns Resolution100 fs Self calibrationSupported – At time of measurement, when temperature or bit rate are changed, instrument will recommendaself calibration. |
| **Trigger output Providesapulse trigger to external test equipment. It has two modes** | Divided Clock Mode: Pulses at 1/256th of the clock rate. |

| PARAMETER | VALUE |
|---|---|
| **Pattern Mode** | Pulse ataprogrammable position in the pattern (PRBS), or fixed location (RAM patterns). Minimum pulse width128 clock periods (Mode 1) 512 clock periods (Mode 2) Transition time<500 ps Output levels>300 mV amplitude, 650 mV offset Interface50 Ω SMA female Error detector rear panel connections Detector start input Used to trigger the acquisition of incoming data into the Error Detector reference pattern memory. High level starts capture. |
| **Bandwidth** | Single-ended to differential input channel for easily adding lowfrequency signal generators to test setups USB control and power with no need for additional external power BSASWITCH instrument switch User interfaces User interfaces take usability to |
| **Rise Time** | Fall time Unit interval (data, and also clock) Eye amplitude Noise level of 1 or 0 Eye width Eye height Eye jitter (p-p and RMS) 0 level, 1 level Extinction ratio Vertical eye closure penalty (VECP) Dark calibration Signal-to-Noise ratioVp-p , V |
| **Data Rate** | range of BERTScope 100 MHz to 2.5 GHz Adjustable in 100 kHz steps Adjustable from 0 to 400 mV Common mode or differential Available from the rear-panel 50 Ω SMA connector, single ended with data amplitude from 0 to 3 V adjustable from GUI, same frequ |
| **Attenuation** | values can be entered to properly scale eye diagrams and measurements when external attenuators are used. |
| **Operating temperature** | range10 °C to 35 °C (50 °F to 95 °F) Operating humidityNoncondensing at 35 °C (95 °F), 15 to 65% CertificationsEU EMC Directive (CE-Marked), LVD Low Voltage Directive, US Listed UL61010-1, Canada Certified CAN/CSA 61010-1 |
| **Warm-up time** | minutes Operating temperature range10 °C to 35 °C (50 °F to 95 °F) Operating humidityNoncondensing at 35 °C (95 °F), 15 to 65% CertificationsEU EMC Directive (CE-Marked), LVD Low Voltage Directive, US Listed UL61010-1, Canada Certified CAN/CSA 61010- |

## Environmental Characteristics

| PARAMETER | VALUE |
| --- | --- |
| **Operating temperature** | range10 °C to 35 °C (50 °F to 95 °F) |
| **Warm-up time** | minutes |

## General Specifications & Supplementary Characteristics

| PARAMETER | VALUE |
| --- | --- |
| **Operating temperature** | range10 °C to 35 °C (50 °F to 95 °F) |
| **Operating Temperature** | range10 °C to 35 °C (50 °F to 95 °F) |
| **Warm-up time** | minutes |
| **All Models Include** | user manual, power cord, mouse, three (3) short low-loss cables<br>BSA125CBERTScope 12.5 Gb/s Bit Error Rate Analyzer<br>BSA175CBERTScope 17.5 Gb/s Bit Error Rate Analyzer<br>BSA286CLBERTScope 28.6 Gb/s Bit Error Rate Analyzer |
| **All Models Include** | user manual, power cord, mouse, three (3) short low-loss cables<br>BSA125CBERTScope 12.5 Gb/s Bit Error Rate Analyzer<br>BSA175CBERTScope 17.5 Gb/s Bit Error Rate Analyzer<br>BSA286CLBERTScope 28.6 Gb/s Bit Error Rate Analyzer |

## Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

performance specifications
Pattern Generation and Error Analysis, High-speed BER
Measurements up to 28.6 Gb/s
Fast Input Rise Time / High Input Bandwidth Error Detector for
Accurate Signal Integrity Analysis
Physical Layer Test Suite with Mask Testing, Jitter Peak, BER Contour, and Q-factor Analysis for
Comprehensive Testing with Standard or
User-defined Libraries of Jitter Tolerance Templates
Integrated Eye Diagram Analysis with BER Correlation
Optional Jitter Map Comprehensive Jitter Decomposition - with Long
Pattern (i.e. PRBS-31) Jitter
Patented Error Location Analysis
™
enables Rapid Understanding of your BER Performance Limitations and Assess Deterministic versus
Random Errors, Perform Detailed Pattern-dependent Error Analysis,
Perform Error Burst Analysis, or Error-free Interval Analysis
Key features
Integrated, calibrated stress generation to address the stressed receiver sensitivity and clock recovery
jitter tolerance test requirements forawide range of standards
Sinusoidal jitter to 100 MHz
Random jitter
Bounded, uncorrelated jitter
Sinusoidal interference
Spread spectrum clocking
PCIe 2.0 & 3.0 receiver testing
F/2 jitter generation for 8xFC and 10GBASE-KR testing
IEEE802.3ba & 32G fibre channel testing
Electrical stressed eye testing for
PCI express
10/40/100 Gb Ethernet
SFP+/SFI
OIF/CEI
Fibre channel (FC8, FC16, FC32)
SATA
USB 3.1
InfiniBand (SDR, QDR, FDR, EDR)
Tolerance compliance template testing with margin testing
Integrated eye diagram analysis with BER correlation
Applications
Design verification including signal integrity, jitter, and timing analysis
Design characterization for high-speed, sophisticated designs
Certification testing of serial data streams and high performance
Networking systems
Design/Verification of high-speed I/O components and systems
Signal integrity analysis – mask testing, jitter peak, BER contour, jitter map, and q-factor analysis
Design/Verification of optical transceivers www.tek.com 1

Linking domains
Eye diagrams have always provided an easy and intuitive view of digital performance. It has been harder to tie this directly with BER performance, as the instruments that provide views of each have been architected in fundamentally different ways. Eye diagrams have been composed of shallow amounts of data that have not easily uncovered rarer events.
BERTs have counted every bit and so have provided measurements based on vastly deeper data sets, but have lacked the intuitive presentation of information to aid troubleshooting.
The BERTScope removes this gap allowing you to quickly and easily view an eye diagram based on at least two orders of magnitude more data than conventional eyes. Seeingafeature that looks out of the ordinary, you are able to place cursors on the item of interest and by simply moving the sampling point of the BERT, use the powerful error analysis capabilities to gain more insight into the feature of interest. For example, check

for pattern sensitivity of the latest rising edges. Alternatively, use one-button measurement of BER Contour to see whether performance issues are bounded or likely to cause critical failures in the field. In each case, information is readily available to enhance modeling or aid troubleshooting, and is available for patterns up to 2
31
- 1 PRBS.
Data rich eye diagrams
As shown previously, there is an impressive difference in data depth between conventional eye diagrams and those taken withaBERTScope.
So what does that mean? It means that you see more of what is really going on - more of the world of low-probability events that is present every time you runalong pattern throughadispersive system of any kind, have random noise or random jitter fromaVCO - a world that is waiting to catch you out when your design is deployed. Adding to this the deeper knowledge that comes from the one-button measurements of BER Contour, Jitter
Peak, and Q-factor, and you can be confident that you are seeing the complete picture.
The BERTScope shown with optical units enabled. In this example measurements are converted to the optical domain automatically.
Deep mask testing
With the ability to vary sample depth, it is very easy to move between deep measurements which giveamore accurate view of the real system performance, and shallow measurements that match those ofasampling oscilloscope. The measurements shown below are from the eye diagram of an optical transmitter. With the BERTScope sample depth set to only
3000 waveforms, the BERTScope generates the diagram shown in the middle in only 1 second. The measured mask margin of 20% exactly correlates to the same measurement made onasampling oscilloscope.
The lower diagram shows the eye produced by the same device, using
Compliance Contour measured ataBER of 1×10
-6
. Here the mask margin is reduced to 17%.
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The depth advantage gained for eye diagrams is at least 10 times greater for mask testing. Unlike pseudo-mask testing offered by some BERTs, a
BERTScope mask test samples every point on the perimeter of an industrystandard mask, including the regions above and below the eye. Not only that, but each point is tested toadepth unseen before. This means that even foratest lastingafew seconds usingamask from the library of standard masks or fromamask you have created yourself, you can be sure that your device has no lurking problems.
Accurate jitter testing to industry standards
Testing with long or short patterns, the most accurate jitter measurement is likely to come from the methodology that uses little or no extrapolation to get its result. With the BERTScope, you can quickly measure to levels of
1×10
-9
(1×10
-10
at high data rates), or wait for the instrument to measure
1×10
-12
directly. Either way, the BERTScope's one-button measurements are compliant to the MJSQ jitter methodology, and because the underlying delay control is the best available on any BERT you can be sure that the measurements are accurate. Use the built-in calculations for Total Jitter (TJ), Random Jitter (RJ), and Deterministic Jitter (DJ), or easily export the data and use your own favorite jitter model.
The BSA286CL's low intrinsic RJ supports serving of 802.3ba's simultaneous VECP (Vertical Eye Closure Penalty) and J2/J9 calibration with valuable margin required to fully characterize 100G Ethernet silicon.
Mask compliance contour testing
Many standards such as XFP/XFI and OIF CEI now specify mask tests intended to assureaspecified 1×10
-12
eye opening. Compliance Contour view makes this easy by takingamask, and overlaying it on your measured BER contours - so you can immediately see whether you have passed the mask at whatever BER level you decide.
Quick selection guide
ModelMaximum bit rateStressed eye - SJ, RJ,
BUJ, SI
BSA286CL28.6 Gb/sOpt. STR
BSA175C17.5 Gb/sOpt. STR
BSA125C12.5 Gb/sOpt. STR
Flexible clocking
The generator clock path features in the BERTScope provides the test flexibility needed for emerging real-

world devices. Whether computer cards or disk drives, it is often necessary to be able to provideasub-rate system clock, such as 100 MHz for PCI Express
®
(PCIe). To get the target card running may requireadifferential clock signal withaparticular amplitude and offset; this is easily accomplished with the BERTScope architecture, with many flexible divide ratios available.
Clock path in BERTScope Option STR models
Spread Spectrum Clocking (SSC) is commonly used in electrical serial data systems to reduce EMI energy by dispersing the power spectrum.
Adjustable modulation amplitude, frequency, andachoice of triangle or sine modulation wave shape allow testing receivers to any compliance standard which utilize SSC. An additional modulator and source allows users to stress the clock with high-amplitude, low-frequency Sinusoidal
Jitter (SJ).
Bit Error Rate Tester -- BERTScope
®
BSA Series www.tek.com 3

Working with closed eyes
With the need to push ever-increasing data rates through electrical channels, the frequency-dependent losses often result in eye closure at the receiver end. Engineers use equalization to compensate for these losses and "open the eyes" in the real system. Tektronix offers powerful tools that allow designers to characterize and test compliance of receiver and transmitter components used in these systems.
In keeping with the BERTScope philosophy, the graphical user interface presents the control functionality inalogical, easy-to-follow format. A time domain representation of the response shows the effects of tap weight settings. The frequency domain Bode plot shows how the filter will compensate for the channel losses.
For receiver testing, the DPP125C Digital Pre-emphasis Processor adds calibrated pre-emphasis to the BERTScope pattern generator outputs, emulating pre-emphasis applied at the transmitter. Pre-emphasis is currently used in 10GBASE-KR, PCIe, SAS 12 Gb/s, DisplayPort
®
, USB
3.1, and other standards.
Features:
1-12.5 Gb/s clock rates
3- or 4-tap versions
Flexible cursor placement allowing pre-cursor or post-cursor
Option ECM (Eye opener, Clock Multiplier, Clock Doubler)
PatternVu
The PatternVu option includesasoftware-implemented FIR filter which can be inserted before the eye pattern display. In systems employing receiver equalization, this allows you to view the eye diagram and perform physical measurements on the eye as the receiver's detector would see it, after the effect of the equalizer. Equalizers with up to 32 taps can be implemented, and the user can select the tap resolution per UI.
PatternVu
PatternVu also includes CleanEye, a pattern-locked averaging system which removes the nondeterministic jitter components from the eye. This allows you to clearly see pattern-dependent effects such as ISI (InterSymbol Interference) which are normally obscured by the presence of high amounts of random jitter.
Single Value Waveform export isacomponent in the PatternVu option. This allows you to captureapattern-locked waveform showing single bits, similar toasingle-shot capture inareal-time oscilloscope. Once captured, the waveform can be exported inavariety of formats for further analysis in an external program.
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Add clock recovery
The Tektronix CR125A, CR175A, and CR286A add levels of flexibility in compliant clock recovery. Most standards requiring jitter measurement specify the use of clock recovery, and exactly which loop bandwidth must be used. Usingadifferent or unknown loop bandwidth will almost certainly give you the wrong jitter measurement. The new clock recovery instrument enables easy and accurate measurements to be made to all of the common standards.
The intuitive user interface provides easy control of all operating parameters. A unique
Loop Response view shows the loop characteristics – actually measured, not just the settings value.
The usefulness of the BERTScope CR is not just confined to BERTScope measurements. Use them stand-alone in the lab with your sampling oscilloscopes, or with existing BERT equipment. Compliant measurements are available to you by pairing either of these versatile instruments with your existing investments.
Display and measure SSC modulation
Spread Spectrum Clocking (SSC) is used by many of the latest serial busses including SATA, PCI Express, and next-generation SAS to reduce
EMI issues in new board and system designs. The Tektronix CR Family provides spread spectrum clock recovery together with the display and measurement of the SSC modulation waveform. Automated measurements include

minimum and maximum frequency deviation (in ppm or ps), modulation rate of change (dF/dT), and modulation frequency. Also included are display of the nominal data frequency and easy-to-use vertical and horizontal cursors.
SSC waveform measurement
Add jitter analysis
CombineaTektronix CR125A, CR175A, or CR286A with Option 12GJ,
17GJ, and 28GJ respectively and your sampling oscilloscope or
BERTScope for variable clock recovery from 1.2 to 11.2 Gb/s, Duty Cycle
Distortion (DCD) measurement, and real-time jitter spectral analysis.
Display jitter spectral components from 200 Hz to 90 MHz with cursor measurements of jitter and frequency.
Measure band-limited integrated jitter with user-settable frequency-gated measurements (preset band limits and integrated jitter measurement for PCI Express 2.0 jitter spectrum in this example).
Bit Error Rate Tester -- BERTScope
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Jitter spectrum measurement
Taking stress out of receiver testing
As networks have changed, so have the challenges of testing receivers.
While tests such as BER and receiver sensitivity are still important, receiver jitter tolerance has evolved to be more real-world for jitter-limited systems such as 10 Gb/s data over back planes and new high-speed buses.
Stressed Eye testing is becoming increasingly common asacompliance measurement in many standards. In addition, engineers are using it to explore the limits of their receiver performance to check margins in design and manufacturing.
Creating the stress recipe for receiver testing toacomplicated standard such as PCIe 2.0 used to require "racking and stacking" several instruments, then spending hours calibrating the setup. With BERTScope, an easy-to-understand graphical view gives you control of all of the calibrated stress sources you need – inside the same instrument.
Eliminating the need for external cabling, mixers, couplers, modulators, etc.
simplifies stress calibration.
Stressed Eye view
Flexible stress impairments
The BERTScope has high-quality, calibrated sources of stress built-in, including RJ, SJ, BUJ, and SI.
ISI is alsoacommon ingredient in many standards. The BSA12500ISI
differential ISI board providesawide variety of path lengths, free from switching suck-outs and anomalies.
Flexible stress impairments
Many standards call for SJ to be stepped throughatemplate with different
SJ amplitudes at particular modulation frequencies. This is easy with the built-in Jitter Tolerance function which automatically steps throughatemplate that you designed, or one of the many standard templates in the library.
Built-in jitter tolerance function
Datasheet


BERTScope pattern generators
The BERTScope pattern generators provideafull range of PRBS patterns, common standards-based patterns, and user-defined patterns.
Option STR provides full integrated, calibrated stress generation which is an easy-to-use alternative toarack full of manually calibrated instruments needed to provideastressed pattern. Uses include receiver testing of devices with internal BER measurement ability such as DisplayPort, or adding stress capability to legacy BERT instruments.
Stressed eye option
Pattern capture
There are several methods for dealing with unknown incoming data. In addition to Live Data Analysis discussed above, a useful standard feature on all BERTScope analyzers is pattern capture. This allows the user to specify the length ofarepeating pattern and then allow the analyzer to grab the specified incoming data using the detector's 128 Mb RAM memory. This can then be used as the new detector reference pattern, or edited and saved for later use.
Pattern capture
Using the Power of Error Analysis – In the following example eye diagram views were linked with BER to identify and solveadesign issue inamemory chip controller. The eye diagram (top left) showsafeature in the crossing region that is unexpected and appearing less frequently than the main eye. Moving the BER decision point to explore the infrequent events is revealing. Error Analysis shows that the features are related in some way to the number 24. Further investigation traced the anomaly to clock breakthrough within the IC; the system clock was at 1/24th of the output data rate. Redesigning the chip with greater clock path isolation gave the clean waveform of the top right eye diagram.

Power of error analysis example
Pattern generator stressed eye
The pattern generator stressed eye function provides the following features:
Flexible, integrated stressed eye impairment addition to the internal or an external clock
Easy setup, with complexity hidden from the user with no loss of flexibility
Verify compliance to multiple standards using the BERTScope and external ISI filters. Standards such as:
OIF CEI
6 Gb SATA
PCI Express
XFI
USB 3.1
SONET
SAS 2
XAUI
10 and 100 Gb Ethernet
DisplayPort
Sinusoidal interference may be inserted in-phase or in anti-phase, or sent externally to be summed after an external ISI reference channel
Sinusoidal jitter may be locked between two BERTScopes in-phase or anti-phase, as required by OIF CEI
Bit Error Rate Tester -- BERTScope
®


Amplitude and ISI impairments
For ISI, add externally: for example, long coaxial cable length, or BesselThompson 4th Order Filter with −3 dB point at 0.75 of bit rate, etc.
For applications requiring circuit board dispersion, the BSA12500ISI
differential ISI accessory board can be used.
Sinusoidal interference
Supports full data rate range of BERTScope
100 MHz to 2.5 GHz
Adjustable in 100 kHz steps
Adjustable from 0 to 400 mV
Common mode or differential
Available from the rear-panel 50 Ω SMA connector, single ended with data amplitude from 0 to 3 V adjustable from GUI, same frequency range and step size as internal adjustment
Jitter measurements
Multi-gigabit serial data channels have eye openings onlyacouple hundred picoseconds wide – or less. In systems where onlyafew picoseconds of jitter count, accurate measurement of jitter is essential for managing tight jitter budgets. The BERTScope has two sets of tools which perform these critical measurements.
The Physical Layer Test Suite option includes measurement of Total Jitter (TJ) along with breakdown into Random Jitter (RJ) and Deterministic Jitter (DJ), using the well-accepted Dual Dirac method. The deep, BERTcollected measurements use several orders of magnitude less extrapolation, or in some cases no extrapolation, than oscilloscopes use asabasis for the jitter measurements. This produces inherently more accurate results than measurements made on other instruments which rely on high levels of extrapolation.
MJSQ-compliant Dual Dirac jitter measurement.
The optional Jitter Map is the latest suite of jitter measurements available for the BERTScope. It providesacomprehensive set of subcomponent analysis beyond RJ and DJ, including many measurements compliant with higher data rate standards. Jitter Map can also measure and decompose jitter on extremely long patterns, such as PRBS-31, as well as live data (requires Live Data Analysis option) providing that it can first run onashorter synchronized data pattern.
Jitter map
Features include:
DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data
Dependent Jitter (DDJ), Inter-Symbol Interference (ISI), Duty Cycle
Distortion (DCD), and Sub-Rate Jitter (SRJ) including F/2 (or F2) Jitter
BER-based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10
−12
BER and beyond
Separation of correlated and non-correlated jitter components eliminates mistaking long pattern DDJ for RJ
Can measure jitter with minimum eye opening
Additional levels of breakdown not available from other instruments such as: Emphasis Jitter (EJ), Uncorrelated Jitter (UJ), Data
Dependent Pulse Width Shrinkage (DDPWS), and Non-ISI
Intuitive, easy-to-navigate jitter tree
Datasheet

Jitter peak and BER contour measurements made on live data.
Flexible external jitter interfaces
Flexible external jitter interfaces include the following features:
Front panel external high frequency jitter input connector – jitter from
DC to 1.0 GHz up to 0.5 UI (max) can be added, of any type that keeps within amplitude and frequency boundaries
Rear panel external SJ low frequency jitter input connector – jitter from
DC to 100 MHz up to 1 ns (max) can be added
Rear panel SJ output
Sinusoidal interference output rear panel connector
The internal RJ, BUJ, and external high-frequency jitter input is limited to
0.5 UI, combined, further limited to 0.25 UI each when both are enabled.
Rear-panel low-frequency jitter input can be used to impose additional jitter; the sum of external low-frequency jitter, internal low-frequency SJ to
10 MHz, PCIe LFRJ and PCIe LFSJ (with Option PCISTR) is limited to
1.1 ns. This limit does not apply to Phase Modulation (PM) from Option
XSSC.
Jitter impairments
Bounded uncorrelated jitter:
Supports data rates from 1.5 to 12.5 Gb/s (BSA125C), 17.5 Gb/s (BSA175C), and 28.6 Gb/s (BSA286CL) with limited performance to
622 Mb/s (BSA286CL excluded)
Internal PRBS Generator
Variable up to 0.5 UI
100 Mb/s to 2.0 Gb/s
Band-limited by selected filters
BUJ rateFilter
100 to 499 25 MHz
500 to 999 50 MHz
1,000 to 1,999 100 MHz
2,000 200 MHz
Random jitter:
Supports data rates from 1.5 to 12.5 Gb/s (BSA125C), 17.5 Gb/s (BSA175C), and 28.6 Gb/s (BSA286CL) with limited performance to
622 Mb/s (BSA286CL excluded)
Variable up to 0.5 UI
Band-limited 10 MHz to 1 GHz
Crest factor of 16 (Gaussian to at least 8 standard deviation or about
1×10
−16
probability)
Sinusoidal jitter
Data rate
Internal SJ frequencyMaximum internal SJ
amplitude
Up to 12.5 Gbps (BSA125C, or 17.5 Gbps (BSA175C)
1 kHz to 10 MHz
1
1100 ps
10 MHz to 100 MHz200 ps
Up to 28.6 Gb/s (BSA286CL)
1 kHz to 100 MHz1100 ps
2
270 ps
3
1
Can be combined with other low-frequency modulation.
2
Full SJ range is 270 ps with RJ or BUJ the range is reduced to 220 ps.
3
Range is selectable between 1100 ps and 270 ps maximum; a lower range has lower intrinsic jitter.
Bit Error Rate Tester -- BERTScope
®


SJ adjustable from 0 to levels greater than or equal to range in table. See
Additional stress options for more SJ capabilities.

Testing interface cards
Finallyasolution to the age-old problem of making physical layer measurements on high-speed line cards, motherboards, and live traffic –
the BERTScope Live Data Analysis option. Through novel use of the dualdecision point architecture, the instrument is able to make parametric measurements such as Jitter, BER Contour, and Q-factor in addition to the eye and mask measurements that are usable as standard – all that is required isaclock signal. Add the Jitter Map option to see even more layers of jitter decomposition on live data. No more frustration because the pattern is not known, is unpredictable, or involves rate-matching word insertions. Troubleshooting is so much easier now that the one-button physical layer tests can be employed to provide unique insight.
Using the USB3 instrument switch
The BSASWITCH Instrument Switch isaflexible device usable for generalpurpose applications and specific inclusion in USB 3.1 compliance testing.
For USB 3.1 testing, the switch featuresapattern generator for generation of Low Frequency Periodic Signaling (LFPS), used to ensure devices achieve loopback. Other features include:
Manual switching between channels with front-panel controls
Automated control through USB
Flexible triggering with multiple control choices
Two main input channels (Ch 1, Ch 2) with >10 GHz analog bandwidth
Single-ended to differential input channel for easily adding lowfrequency signal generators to test setups
USB control and power with no need for additional external power
BSASWITCH instrument switch
User interfaces
User interfaces take usability to new heights:
Easy navigation
Logical layout and operation
Multiple ways of moving between screens
Relevant information right where you need it
Color coding to alert you to the presence of nonstandard conditions
UI setup screens
Use the Editor screen for pattern editing of standard and AB page select patterns and mask editing and other tasks:
Views in Binary, Decimal, or Hexadecimal
Support for variable assignments, repeat loops, seeding of PRBS
patterns
Capture and editing of incoming data – for example, to makearepeating pattern out of real-world traffic
Capture is available by trigger, by length, or by length followingatrigger
Capture is by number or words, 1 word is 128 bits. For example, a
PRBS-7 (127 bits long) would be captured as 127 words, and would have overall length of 16,256 bits


Editor screen
BERTScope built-in parametric measurements
All BERTScopes come with eye diagrams and mask test capabilities as standard, along with error analysis.
Eye diagrams:
280×350 pixel waveform display
Deep acquisition
Automatic Measurements include:
Rise time
Fall time
Unit interval (data, and also clock)
Eye amplitude
Noise level of 1 or 0
Eye width
Eye height
Eye jitter (p-p and RMS)
0 level, 1 level
Extinction ratio
Vertical eye closure penalty (VECP)
Dark calibration
Signal-to-Noise ratioVp-p
, V
max
, V
min
, crossing levels
Rising and falling crossing level (picoseconds)

Overshoot 0 level and 1 level
Average voltage/power
Cross amplitude, noise level 1 or 0, voltage
Optical modulation amplitude (OMA)
Sample count
Offset voltage
De-emphasis ratio
Mask testing:
Library of standard masks (such as, XFP, or edit custom masks)
Addition of positive or negative mask margin
Import of measured BER contour to become process control mask
At least 1000x the sample depth of traditional sampling oscilloscope masks is ideal for ensuring the absence of rare event phenomena
Optical units:
An external optical receiver can be added to the input of the BERTScope detector. Through the user interface it is easy to input and save the characteristics of the receiver. Once accomplished, relevant units on physical layer displays are changed to optical power in dBm, µW, or mW. Coupling can be AC or DC, and the software steps the user through dark calibration.
For electrical signals, attenuation values can be entered to properly scale eye diagrams and measurements when external attenuators are used.
Variable-depth eye and mask testing:
For eye diagrams and mask testing, the depth of test may be varied in manual mode; the instrument will take the specified number of waveforms then stop. The range is 2,000 to 1,000,000 bits (complete waveforms). Alternatively, the default mode is Continuous, and the eye or mask test increases in depth over time.
Physical layer test option
The following physical layer test options are available:
BER contour testing
Executed with same acquisition circuitry as eye diagram measurements for maximum correlation
As-needed delay calibration for accurate points
Automatic scaling, one-button measurement
Extrapolates contours from measured data, increasing measurement depth with run time and repeatedly updating curve fits
Easy export of fitted data in CSV format
Contours available from 10
−6
to 10
−16
in decade steps
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Basic jitter measurements
Testing to T11.2 MJSQ BERTScan methodology (also called ‘Bathtub Jitter’)
Deep measurements for quick and accurate extrapolation of Total Jitter at user-specified level, or direct measurement
Separation of Random and Deterministic components, as defined in MJSQ
As-needed delay calibration for accurate points
Export of points in CSV format
Easy one-button measurement
User-specified amplitude threshold level, or automatic selection
Selectable starting BER to increase accuracy when using long patterns, as defined in MJSQ
Q-factor measurement
One-button measurement ofavertical cross section through the middle of the eye
Easy visualization of system noise effects
Export of data in CSV format
Compliance contour
Validation of transmitter eye performance to standards such as XFP/XFI and OIF CEI
Overlay compliance masks onto measured BER contours and easily see whether devices pass the BER performance level specified
Live data analysis option
The Live data analysis option is designed to measure parametric performance of traffic that is either unknown or non-repeating. This can include traffic with idle bits inserted, such as, in systems with clock rate matching. It is also suitable for probing line cards.
The option uses one of the two front-end decision circuits to decide whether each bit isaone or zero by

placing it in the center of the eye. The other is then used to probe the periphery of the eye to judge parametric performance. This method is powerful for physical layer problems, but will not identify logical problems due to protocol issues, whereazero was sent when it was intended to beaone.
Live data measurements can be made using BER Contour, Jitter Peak,
Jitter Map, and Q-factor. Eye diagram measurements can be made on live data without the use of this option, providingasynchronous clock is available.
The Live data analysis option requires the Physical layer test option and must be used withafull-rate clock.
PatternVu equalization processing option
PatternVu
4
adds several powerful processing functions to the BERTScope:
CleanEye is an eye diagram display mode, which averages waveform data to present an eye diagram with the non-data-dependent jitter removed. This allows the user to view and measure data-dependent jitter such as Inter-Symbol Inference, giving an intuitive idea of the compensatable jitter present, for example. It is effective on any repeating pattern up to 32,768 bits long.
Single value waveform export isautility which converts the CleanEye output to an export file in Comma Separated Vector (CSV) format. The output file, of up to 105 bit points, can then be imported into Microsoft Excel or software analysis and simulation tools such as Stateye or
MATLAB
®
. This allows offline filtering of real captured data and the implementation of standards-based processing such as Transmitter
Waveform Dispersion Penalty (TWDP) required by 802.3aq, the recent
Long Reach MultiMode (LRM) 10 Gb Ethernet standard.
The FIR filter equalization processor allows the emulation of the communication channel to view and measure the eye as the detector in the receiver would, by applyingasoftware linear filter to the data before it is displayed. For example, the FIR Filter can be used to emulate the lossy effects ofabackplane channel, or alternatively, emulate the receiver’s equalization filter, facilitating the design and characterization of receiver-side equalization.
The filter characteristics are controlled by entering the individual weighting coefficients ofaseries of taps in the FIR filter. Up to 32 taps with tap spacing from 0.1 to 1.0 unit intervals (UI) can be programmed to allow fine resolution of the filter shape. The FIR Filter can be applied to repeating patterns up to 32,768 bits long.
Single edge jitter measurement allows truly deep BER-based jitter measurements to be applied to individual data edges at data rates above 3 Gb/s. The Single Edge Jitter Peak measurement function enables computation of jitter onauser-selectable single edge in the pattern, for repeating patterns up to 32,768 bits long. The resulting jitter measurement excludes data-dependent effects, showing only the uncorrelated jitter components such as Random Jitter (RJ), Bounded
Uncorrelated Jitter (BUJ), and Periodic Jitter (PJ).
Flexible measurements enables users to specify exactly the portion of the CleanEye waveform to use for accurate measurement of amplitude, rise and fall time, and de-emphasis ratio. Preprogrammed formulas for standards such as PCI Express and USB 3.1 are included.
4
PatternVu operates at data rates of 900 Mb/s and higher.


Error analysis
Error analysis isapowerful series of views that associate error occurrences so that underlying patterns can be easily seen. It is easy to focus in onaparticular part of an eye diagram, move the sampling point of the BERTScope there, and then probe the pattern sensitivity occurring at that precise location. For example, it is straightforward to examine which patterns are responsible for late or early edges.
Many views come standard with the BERTScope Family:
Error statistics: A tabular display of bit and burst error counts and rates
Error Statistics view showing link performance in terms of bit and burst occurrences.
Strip chart: A strip chart graph of bit and burst error rates
Strip Chart view showing bit and burst error performance over time. This can useful while temperature cycling as part of troubleshooting.

## Specifications

| PARAMETER | VALUE |
| --- | --- |
| **Burst length** | A histogram of the number of occurrences of errors of different lengths |

| PARAMETER | VALUE |
|---|---|
| **Error free interval** | A histogram of the number of occurrences of different error-free intervals |
| **Correlation** | A histogram showing how error locations correlate to userset block sizes or external marker signal inputs |
| **Pattern sensitivity** | A histogram of the number of errors at each position of the bit sequence used as the test pattern |
| **Block errors** | A histogram showing the number of occurrences of data intervals (ofauser-set block size) with varying numbers of errors in them |

The Pattern Sensitivity view isapowerful way of examining whether error events are pattern related. It shows which pattern sequences are the most problematic, and operates on PRBS and user-defined patterns.
Error analysis options
Forward error correction emulation
Because of the patented error location ability of the BERTScope, it knows exactly where each error occurs duringatest. By emulating the memory blocks typical of block error correcting codes such as Reed-Solomon architectures, bit error rate data from uncorrected data channels can be passed through hypothetical error correctors to find out whataproposed
FEC approach would yield. Users can set up error correction strengths, interleave depths, and erasure capabilities to match popular hardware correction architectures.
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BSA Series www.tek.com 13

2-D error mapping
This analysis createsatwo-dimensional image of error locations from errors found during the test. Error mapping based on packet size or multiplexer width can show if errors are more prone to particular locations in the packet or particular bits in the parallel bus connected to the multiplexer. This visual tool allows for human eye correlation, which can often illuminate error correlations that are otherwise very difficult to find –
even with all the other error analysis techniques.
Error location capture
CharacteristicDescription
Live analysisContinuous
Error logging capacityMaximum 2 GB file size
Error events/second10,000
Maximum burst length32 kb
Jitter tolerance template option
Many standards call for SJ to be stepped throughatemplate with different
SJ amplitudes at particular modulation frequencies. This is easy with the built-in Jitter Tolerance function which automatically steps throughatemplate that you designed, or one of the many standard templates in the library.
Standard library of templates:
10GBASE LX4 802.3ae 3.125 Gb/s
10 GbE 802.3ae 10.3125 Gb/s
40 GbE 802.3ba LR4 10.3125 Gb/s
100 GbE 802.3ba LR4/ER4 25.78125 Gb/s
CEI 11G Datacom Rx Ingress (D) 11 Gb/s
CGE Telecom Rx Egress (Re) 11 Gb/s
5
CEI 11G Telecom Rx Ingress (Ri) 11 Gb/s
5

## Specifications

| PARAMETER | VALUE |
|---|---|
| **CEI 11G Total Wander 11.1 Gb/s** | CEI 11G Total Wander 9.95 Gb/s |
| **CEI 6G Total Wander 4.976 Gb/s** | CEI 6G Total Wander 6.375 Gb/s |

| PARAMETER | VALUE |
| --- | --- |
| **CEI 25G Total Wander 25.78125 Gb/s** | FBB DIMM1 3.2 Gb/s |
| **FBB DIMM1 4.0 Gb/s** | FBB DIMM1 4.8 Gb/s |
| **FBB DIMM2 3.2 Gb/s** | FBB DIMM2 4.0 Gb/s |
| **FBB DIMM2 4.8 Gb/s** | Fibre Channel 1.0625 Gb/s |
| **Fibre Channel 2.125 Gb/s** | Fibre Channel 4.25 Gb/s |
| **Fibre Channel 8G 8.5 Gb/s** | Fibre Channel 16G 14.025 Gb/s |

OTN OTU-1 2.666G
5
OTN OTU-2 10.709 Gb/s
OTN(10BASE-R) 11.1 Gb/s
SAS (SCSI) 1.5 Gb/s
SAS (SCSI) 3 Gb/s
SDH 0.172 STM-1 155M
5
SDH 0.172 STM-16 2.4832 Gb/s
5
SDH 0.172 STM-4 622 Mb/s
5
SDH 0.172 STM-64 9.956 Gb/s
5
SDH STM-16 2.48832 Gb/s
5
SDH STM-64 9.9532 Gb/s
5
SONET OC-48 2.48832 Gb/s
5
SONET OC12 622 Mb/s
5
SONET OC192 9.9532 Gb/s
5
SONET OC192 9.95 Gb/s
5
SONET OC3 155 Mb/s
5
SONET OC48 2.4832 Gb/s
5
USB 3.1 5 & 10 Gb/s
XAUI 3.125 Gb/s
XFI ASIC Rx In Datacom (D) 10.3125 Gb/s
XFI ASIC Rx In Datacom (D) 10.519 Gb/s
XFI ASIC Rx In Telecom (D) 10.70 Gb/s
XFI ASIC Rx In Telecom (D) 9.95328 Gb/s
5
XFI Host Rx In Datacom (C) 10.3125 Gb/s
XFI Host Rx In Datacom (C) 10.519 Gb/s
XFI Host Rx In Telecom (C) 10.70 Gb/s
5
XFI Host Rx In Telecom (C) 9.95328 Gb/s
5
XFI Module Tx In Datacom (B') 10.3125 Gb/s
XFI Module Tx In Datacom (B') 10.519 Gb/s
XFI Module Tx In Telecom (B') 10.70 Gb/s
5
XFI Module Tx In Telecom (B') 9.95328 Gb/s
5
5
Requires Option XSSC.

Some of the areas of adjustment include:
BER confidence level
Test duration per point
BER threshold
Test device relaxation time
Imposition of percentage margin onto template
Test precision Control over A/B Pattern switch behavior
Also included is the ability to test beyond the template to device failure at each chosen point, and the ability to export data either as screen images or
CSV files.
Jitter map option
The Jitter map
6
option provides automated jitter decomposition with long pattern jitter triangulation. It extends BER-based jitter decomposition beyond Dual Dirac measurement of Total Jitter (TJ), Random Jitter (RJ), and Deterministic Jitter (DJ) toacomprehensive set of subcomponents. It can also measure and decompose jitter on extremely long patterns, such as PRBS-31, providing that it can first run onashorter synchronized data pattern.
The option includes the following features:
DJ breakdown into Bounded Uncorrelated Jitter (BUJ), Data
Dependent Jitter (DDJ), Inter-Symbol Interference (ISI), Duty Cycle
Distortion (DCD), and Sub-Rate Jitter (SRJ)
7
including F/2 (or F2) jitter
BER based for direct (non-extrapolated) Total Jitter (TJ) measurement to 10
−12
BER and beyond
Separation of correlated and uncorrelated jitter components eliminates mistaking long pattern DDJ for RJ
Visualization of RJ RMS measured on individual edges of the data pattern
J2 and J9 jitter measurements for 100 GbE applications
Additional levels of breakdown not available from other instruments such as: Emphasis Jitter (EJ), Uncorrelated Jitter (UJ), Data
Dependent Pulse Width Shrinkage (DDPWS), and non-ISI
Intuitive, easy-to-navigate jitter tree
Stressed live data option
The BERTScope Stressed Live Data software option enables engineers to add various types of stress to real data traffic in order to stress devices with bit sequences representative of the environment they will encounter once deployed. Using live traffic with added stress tests the boundaries of device performance and lends added confidence to designs before they are shipped.
Full range of calibrated stress available on the BERTScope, including
Sinusoidal Jitter (SJ), Random Jitter (RJ), Bounded Uncorrelated Jitter (BUJ), Sinusoidal Interference (SI), F/2 Jitter, and Spread Spectrum
Clocking (SSC)
Data rate support up to the maximum of the BERTScope
Full-rate clock required up to 11.2 Gb/s, half-rate clock required above
11.2 Gb/s
Symbol filtering option
Symbol filtering enables asynchronous BER testing, including Jitter
Tolerance testing, on incoming data streams that haveanondeterministic number of clock compensation symbols inserted into the bit stream, as is common in 8b/10b encoded systems when placed in loopback for receiver testing.
Supports asynchronous receiver testing for USB 3.1, SATA, and PCI
Express
User-specified symbols are automatically filtered from the incoming data to maintain synchronization
The Error Detector maintainsacount of filtered bits for accurate BER
measurement
6
Jitter map operates at data rates of 900 Mb/s and higher.
7
SRJ and F/2 jitter operate up to 11.2 Gb/s (BSA125C, BSA175C, BSA286CL).
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Pattern generator specifications
All specifications are guaranteed unless noted otherwise. All specifications apply to all models unless noted otherwise.
Data outputs
Data rate range
BSA125C0.1 to 12.5 Gb/s
BSA175C0.5 to 17.5 Gb/s
BSA286CL1 to 28.6 Gb/s
FormatNRZ
PolarityNormal or inverted
Variable cross over25 to 75%
Patterns
Hardware patternsIndustry-standard Pseudo-random (PRBS) of the following types: 2 n − 1 where n = 7, 11, 15, 20, 23, 31
RAM patterns128 bits to 128 Mb total, allocated in 32 Mb portion

## Ordering Information

| OPTION | DESCRIPTION |
|---|---|
| **Opt. J** | MAPAdd Jitter Decomposition SW |
| **Opt. 4T4** | Tap Digital Pre-emphasis Processor |

### Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: N/A — off-catalog OEM datasheet. See OEM documentation · Not listed on Aumictech inventory.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

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