Aumictech
Test & measurement · bought, sold, repaired, calibrated

Data Sheet
August 13, 2026

TEKTRONIX

Tektronix DPP125C Digital Pre-emphasis Processor

Tektronix DPP125C Digital Pre-emphasis Processor (BERTScope) The Tektronix BERTScope DPP125C isanonlinear signal conditioner that adds controllable digital pre-emphasis / de-emphasis to serial data for hardware equalization, receiver stress, and standards compliance testing. It accepts single-ended SMA clock and data inputs and producesadifferential SMA data output withaclocked 3-tap FIR (optional 4-tap) over 1–12.5 Gb/s. The Tektronix BERTScope DPP125C isanonlinear signal conditioner that adds controllable digital pre-emphasis / de-emphasis to serial data for hardware equalization, receiver stress, and standards compliance testing. It accepts single-ended SMA clock and data inputs and producesadifferential SMA data output withaclocked 3-tap FIR (optional 4-tap) over 1–12.5 Gb/s.

MODEL **Tektronix DPP125C**	CALIBRATION **Available on request**
CONDITION **Used**	STATUS **In stock**
RFQ / SKU **DPP125C**	LISTING **https://aumictechlabs.com/products/dpp125c-2/**

NIST-traceable cal · SAM registered · 30-day returns

NAICS 423690 · 811210 · 541380

This unit

The Tektronix DPP125C Digital Pre-emphasis Processor compensates for signal degradation in high-speed digital communication systems by applying controllable pre-emphasis to enhance signal integrity. It corrects transmission channel impairments through configurable tap-based

equalization, enabling accurate data recovery at the receiver and supporting compliance testing across multiple industry standards. The instrument operates as either a standalone device controlled remotely or integrates fully with a BERTScope for unified software control.Technical Specifications Data Rate: 1 to 12.5 Gb/s Pre-emphasis Configuration: 3-tap or optional 4-tap Supported Standards: 802.3ap, Serial Attached SCSI (SAS), 10GBASE-KR Backplanes, DisplayPort™, USB 3.0/3.1, PCI Express® Gen3 Signal Adjustment: Pre-cursor or post-cursor compensation for inter-symbol interference (ISI) and signal loss mitigation Input Type: Single-ended data and clock inputs Control Methods: Direct tap weight entry, time-domain step response visualization, frequency-domain Bode plot analysis Optional ECM Features: Reference clock multiplication (2.5 GHz, 5 GHz, 8 GHz PCIe compliance), eye opener functionality, 12 Gb/s SAS clock doubler Interfaces: RS-232 for PCIe receiver equalization link training, USB for PC control Clock/Data Delay: Internally compensated for length-matched cables when integrated with BERTScopeKey Features Adjustable tap weights for optimizing compensation across varying channel conditions Amplitude-weighted time-domain bitmap display for step response visualization Frequency-domain Bode plot for monitoring implemented equalization effects Compact footprint compatible with BERTScope stacking geometry Dual operation modes: standalone PC control or full BERTScope integrationTypical Applications Design characterization for high-speed digital systems Certification testing of serial data streams against industry standards High-speed I/O component and system verificationCompatibility & Integration Operated standalone via remote PC or fully integrated with Tektronix BERTScope using BERTScopePC software and drivers.

Features & description

From manufacturer datasheet

Features

• Data rate 1–12.5 Gb/s • Standard 3-tap clocked FIR; Opt. 4T adds fourth tap • Tap weights −100% to +100% in 1% steps (or 0.1 dB) • UI: tap weights, amplitude-weighted step response, Bode plot • USB 2.0 control; AC-coupled data path with DC-coupled output offset • Opt. ECM: PCIe-compliant clock multiplication / eye opener / SAS clock doubler

Applications

• High-speed serial Tx equalization emulation • PCI Express, USB 3.0, SAS, DisplayPort, 10GBASE-KR stress / compliance • Counteracting channel ISI with measured frequency response • BERTScope and stand-alone pattern-generator setups

DPP125C Characteristics / Specifications

PARAMETER	VALUE
Model	DPP125C
Manufacturer	Tektronix
Instrument Type	Digital Pre-emphasis Processor
Product Family	BERTScope DPP Series
Data Rate Range	1–12.5 Gb/s
FIR Function	3-tap clocked FIR (standard); 4-tap with Opt. 4T
Tap Range	−100 to +100 (including 0) in 1% steps
Tap Resolution	1% or 0.1 dB, any tap
Clock Input	Single-ended SMA
Clock Sensitivity Typical	250 mV
Clock Termination	50 Ω, AC coupled
Data Input	Single-ended SMA
Data Sensitivity Typical	250 mV (PN31 pattern)
Data Input Termination	50 Ω, AC coupled
Max Jitter Transfer Clock to Output	1:1
Data Output	Differential SMA
Max Output Amplitude Typical	1.8 V differential, adjustable
Differential Skew Typical	<2 ps
Max DC Offset Typical	±500 mV
Output Coupling	AC-coupled data with DC-coupled output offset
Additive Random Jitter Typical	<350 fs RMS (1010 pattern)
Transition Time	<40 ps, all taps, 1010 pattern
Control Interface	USB 2.0
Weight	4 kg (9 lb)
Power Consumption	<150 W

PARAMETER	VALUE
AC Mains	100–240 V AC, 45–63 Hz, auto-range
Opt. ECM	PCIe-compliant clock multiplication / eye opener / SAS clock doubler
Data Rate	1–12.5 Gb/s - Standard 3-tap clocked FIR; Opt. 4T adds fourth tap - Tap weights −100% to +100% in 1% steps (or 0.1 dB) - UI: tap weights, amplitude-weighted step response, Bode plot - USB 2.0 control; AC-coupled data path with DC-coupled output offse

Full OEM specifications

Complete technical content extracted from the manufacturer datasheet. Sparse OEM tables are reconstructed as tables below; other text is preserved as paragraphs.

Specifications

Specifications

PARAMETER	VALUE
Model	DPP125C
Manufacturer	Tektronix
Instrument Type	Digital Pre-emphasis Processor
Product Family	BERTScope DPP Series
Data Rate Range	1–12.5 Gb/s
FIR Function	3-tap clocked FIR (standard); 4-tap with Opt. 4T
Tap Range	–100 to +100 (including 0) in 1% steps
Tap Resolution	1% or 0.1 dB, any tap
Clock Input	Single-ended SMA
Clock Sensitivity Typical	250 mV
Clock Termination	50 Ω, AC coupled
Data Input	Single-ended SMA
Data Sensitivity Typical	250 mV (PN31 pattern)
Data Input Termination	50 Ω, AC coupled
Max Jitter Transfer Clock to Output	1:1
Data Output	Differential SMA
Max Output Amplitude Typical	1.8 V differential, adjustable
Differential Skew Typical	<2 ps
Max DC Offset Typical	±500 mV
Output Coupling	AC-coupled data with DC-coupled output offset
Additive Random Jitter Typical	<350 fs RMS (1010 pattern)
Transition Time	<40 ps, all taps, 1010 pattern
Control Interface	USB 2.0

Dimensions W×H×D: 39.4 × 9.5 × 33.6 cm

Specifications

PARAMETER	VALUE
Weight	4 kg (9 lb)
Power Consumption	<150 W
AC Mains	100–240 V AC, 45–63 Hz, auto-range

Option 4T: Optional 4-tap processor
Option ECM: PCIe clock multiplication 2.5/5/8 GHz; eye opener; 12 Gb/s SAS clock doubler

Notes
Specs from Tektronix DPP125C / BERTScope Digital Pre-emphasis Processor datasheet. Confirm installed options (4T, ECM) and firmware on the unit.

Ordering Information

OPTION	DESCRIPTION
Opt. ECM	PCIe-compliant clock multiplication / eye opener / SAS clock doubler

Available from Aumictech

Used and refurbished unit evaluated in-house. Calibration: Available on request. Used · In stock.

Request a quote: **sales@aumictech.com** · +1 (484) 841-9341

Aumictech
788 S 500 E, Pleasant Grove, UT 84062
sales@aumictech.com · +1 (484) 841-9341
https://aumictechlabs.com

NIST-traceable calibration · SAM registered · 30-day returns
NAICS 423690 · 811210 · 541380
Generated August 13, 2026